A DIGITAL SPREAD SPECTRUM MODEM FOR VOICE/DATA

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by
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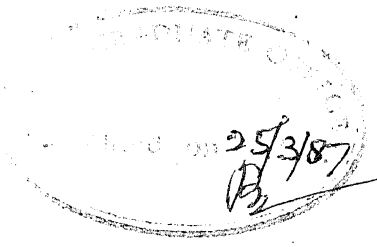

CERTIFICATE

Certified that this work 'A DIGITAL SPREAD SPECTRUM MODEM FOR VOICE/DATA' by P.K. SHARMA has been carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

Spread spectrum techniques permit low probability of intercept and jam resistant communication. Additional attributes of spread spectrum communications include selective calling, identification, multipath protection and accurate time of arrival measurement. In this thesis, fabrication of a MODEM (modulator/demodulator) for Voice/Data modulated spread spectrum system is reported. The system employing Direct Sequence Modulation technique has been fabricated to work at 1.0 M bits/sec. The input to the system is a (0-4) KHz speech signal. This data stream is first pulse code modulated to 66.66 KHz data and then 15 bit pseudo random binary sequence is modulo-2 added. A synchronizing bit is added in the pulse code modulated data to reduce the receiver complexity. The system has been tested for its performance. Suggestion for fault detection and performance measurement of parameters of the system using additional hardware is proposed.

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CHAPTER 1

INTRODUCTION

Digital communication has become increasingly attractive over the past decade both because of increased demand for data communication and digital transmission offers options and flexibility not available with analog transmission. Digital communication involves the transmission of discrete symbols over a potentially noisy channel. Although the physical channel itself (wire, cable, RF channel) is analog, use of digital transmission has a number of advantages compared with traditional analog modulations (AM, FM, SSB) or the sampled analog modulations (PPM, PAM). In analog transmission a varying continuous voltage (or current) is transmitted to a receiver, the receiver attempts to track the original information waveform with as high a fidelity as possible. The effectiveness measure for analog signalling is the output signal to noise ratio where noise is the mean square error between input and output waveform. For digital signalling, where one decides which of a finite set of signals was sent, the primary effectiveness measure is symbol probability of error.

Digital techniques enhance transmission capability. Extremely broadband transmission media such as optical fibre and millimeter wave guides are now available. Extremely low usage of subscriber lines can be improved by digital multiplexing. Data of various speeds can be transmitted much more efficiently by digital transmission compared with its analog counterpart. Speech, data and video signals for the customers, as well as control and supervisory signals for setting up and releasing connections through the network, can be transmitted by digital techniques in an unified stream.

Moreover digital techniques permit signal processing and efficient signal handling. Coding of analog signals permits digital processing to drastically reduce redundancy. Digital information can be temporarily stored without distortion in digital memories which are rapidly becoming inexpensive. The temporary store permits more efficient use of network facilities and provides a variety of buffering benefits such as refreshing and speed conversion.

A major advantage of the digital signalling is that regenerative repeaters can be used in the channel. Analog repeaters consists of amplifiers which amplify any accumulated noise equally along with the signal. The digital

regenerative repeater, on the other hand, reconstructs the signal at each repeater hence channel induced distortion or noise is removed at each repeater.

Digital circuit provides a drastic reduction in hardware cost, extremely high reliability and maintenability and substantial savings in space, material and energy.Progress in integrated circuit technology is cutting down the cost of digital hardware as well as the failure rate of components.

Pulse amplitude modulation and pulse time modulation both suffer from transmission distortion and noise to an appreciable extent, and are therefore not used that often for direct transmission, but more often as intermediate steps in the generation of pulse code modulation. In the PCM system, groups of pulses or codes are transmitted which represents binary numbers corresponding to modulating voltage levels. Recovery of the transmitted information does not depend on the height, width or energy content of the individual pulses, but only on their presence or absence. Since it is relatively easy to recover pulses under these conditions, even in the presence of large amounts of distortion and noise, PCM system tends to be very immune to interference and noise. Regeneration of the pulses on route is also relatively easy, resulting

in a system that produces excellent results for long distance communication.

The average probability of error in a PCM receiver depends solely on the ratio of the peak pulse power to the average noise power, measured at the decoder input in the receiver. As shown in Fig. 1.1, the error probability P_e decreases very rapidly as the peak pulse to noise ratio is

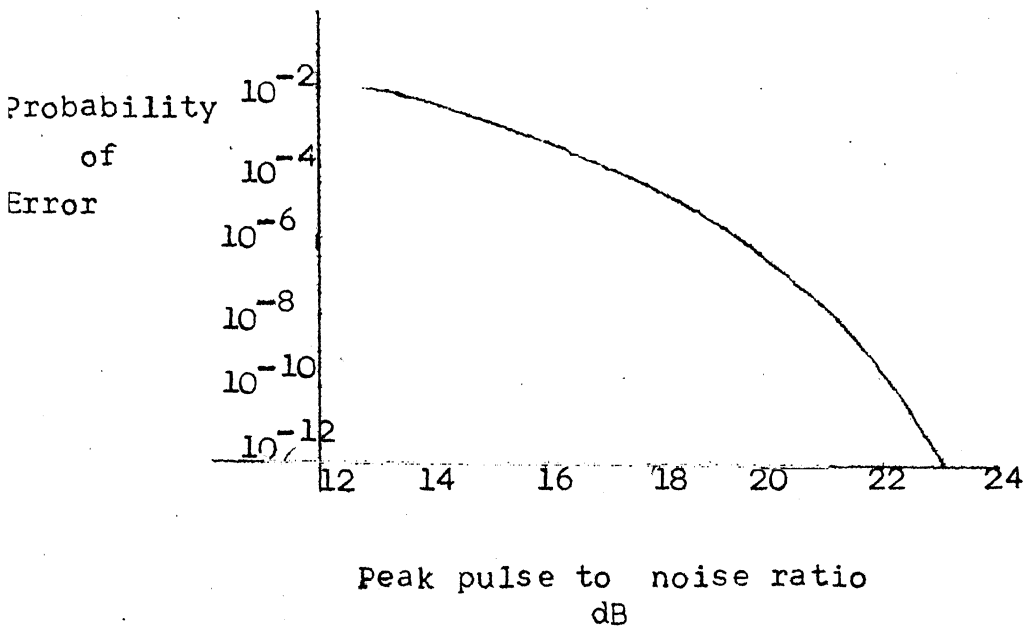

Fig. 1.1: Probability of error in PCM Receiver

increased, so that eventually a very small increase in transmitted pulse power will make the reception of binary pulses almost error free [1]. There is an error threshold (at about 20 dB) below which the receiver performance may involve

significant numbers of errors, and above which the effect of transmission noise is practically negligible. In other words, provided that peak pulse to noise ratio exceeds the error threshold, transmission noise has virtually no effect on the receiver performance, which is precisely the goal of PCM.

Comparing the figure of 20 dB for the error threshold in a PCM system with the 60-70 dB required for high quality transmission of speech using amplitude modulation, hence PCM requires much less power, even though the average noise power in the PCM system is increased by the n-fold increase in bandwidth, where n is the number of bits in a code word.

Another important characteristic of a PCM system is its ruggedness to interference. It has been found that transmission noise in PCM system, using on-off signalling, produces no effect unless the peak amplitude is greater than half the pulse height. Similarly, interference caused by stray impulses or crosstalk will produce no effect unless the peak amplitude of this interference plus noise is greater than half the pulse height. If an adequate margin over the error threshold is provided in the first place, the system can withstand the presence of relatively large amounts of interference [2].

A spread spectrum system is further used for bandwidth expansion of PCM signal because of its numerous advantages. Spread spectrum signals used for the transmission of digital information are distinguished by the characteristic that their bandwidth W is much greater than the information rate R in bits per second. The large redundancy inherent in spread spectrum signals is required to overcome the severe levels of interference that are encountered in the transmission of digital information.

A second important element employed in the design of spread spectrum signals is pseudo randomness, which makes the signal appear similar to random noise and difficult to demodulate by receivers other than the intended ones. This element is intimately related with the application or purpose of such signals.

To be specific, spread spectrum signals have got other advantages such as (1) combating or suppressing the determental effects interference due to jamming, interference arising from other users of the channel, and self interference due to multipath propagation, (2) hiding a signal by transmitting it at a low power and, thus, making it difficult for an unintended listener to detect in the presence of background noise, and (3) achieving message privacy in the presence of other listeners.

In combating intentional interference (Jamming), it is important to the communicators that the jammer which is trying to disrupt the communication does not have proper knowledge of the signal characteristic except for the overall channel bandwidth and the type of modulation being used. If the digital information is just encoded, a sophisticated jammer can easily mimic the signals emitted by the transmitter and, thus, confuse the receiver. To circumvent this possibility the transmitter introduces an element of randomness (pseudo-randomness) in each of the transmitted coded signal waveforms which is known to the intended receiver but not to the jammer.

Interference from other users arises in multiple access communication systems in which a number of users share a common channel bandwidth. At any given time, a subset to these users may transmit information simultaneously over the common channel to corresponding receivers. Assuming that all the users employ the same code for the encoding and decoding of their respective information sequences, the transmitted signals in this common spectrum may be distinguished from one another by super-imposing a different pseudo random pattern, also called a code, in each transmitted signal. Thus a particular receiver can recover the transmitted information intended for it knowing the pseudo random pattern i.e., the key, used by the

corresponding transmitter. This type of communication technique which allows multiple users to simultaneously use a common channel for transmission of information, is called code division multiple access [3].

Resolvable multipath components resulting from time dispersive propagation through a channel may be viewed as a form of self interference. This type of interference may also be suppressed by the introduction of a pseudo random pattern in the transmitted signal.

A signal may be hidden in the background noise by spreading its bandwidth with coding and transmitting the resultant signal at a low average power. Because of its low power level, the transmitted signal is said to be 'covert'. It has a low probability of being intercepted (detected) by a casual listener and hence, is also called a low probability of intercept signal.

Finally, message privacy may be obtained by superimposing a pseudo random pattern on a transmitted message. The message can be demodulated by the intended receivers that know the pseudo-random pattern or key used at the transmitter but not by any other receivers that do not have knowledge of the key.

1.1 DIGITAL SIGNAL MODULATION:

The advantages of coding a signal digitally are efficient signal regeneration, ruggedness, easy encryption, the possibility of combining transmission and switching functions, and a uniform format for different types of signal. The price paid to have these advantages is the increased bandwidth.

Straightforward waveform coding still proves to be an important subject on two counts. First, from the point of view of coder complexity waveform approximating techniques are the most likely candidates for wide scale applications of digital speech coding. Secondly waveform quantization, is, after all, the most generally applicable approach to signal coding. Thus the PCM, DPCM and DM coders are appropriate to the communication of any band limited time function.

While signal to noise (SNR) is still the single most informative measure of quantizer performance, the choice of a specific signal quantizer for a given application should, wherever possible, follow a consideration of how well a coder can reproduce signal perceptually.

In the present thesis pulse code modulation is used which involves the following steps:

a) The band limited waveform is sampled at a rate of at least 2W Hz (the Nyquist frequency), where W is the highest frequency contained in the waveform. Such sampling insures perfect reconstruction of the analog signal by an appropriate subsequent desampler. Also, the minimum sampling rate can be less than 2W if the lowest signal frequency is non-zero.

b) The amplitude of each signal sample is quantized into one of 2^B levels. This implies an information of B bits per sample, and an overall information rate of 2WB bits per second for a low pass filtered signal.

c) The discrete amplitude levels are represented by distinct binary words of length B. For example with B=2, one can represent 4 distinct levels using the code words 00, 01, 10 and 11.

d) For decoding, the binary words are mapped back into amplitude levels, and the amplitude time pulse sequence is low pass filtered with a filter whose cut off frequency is W.

Let the quantizer step size be denoted by Δ . If the number of quantizer levels is large, the quantization has the following uniform distribution:

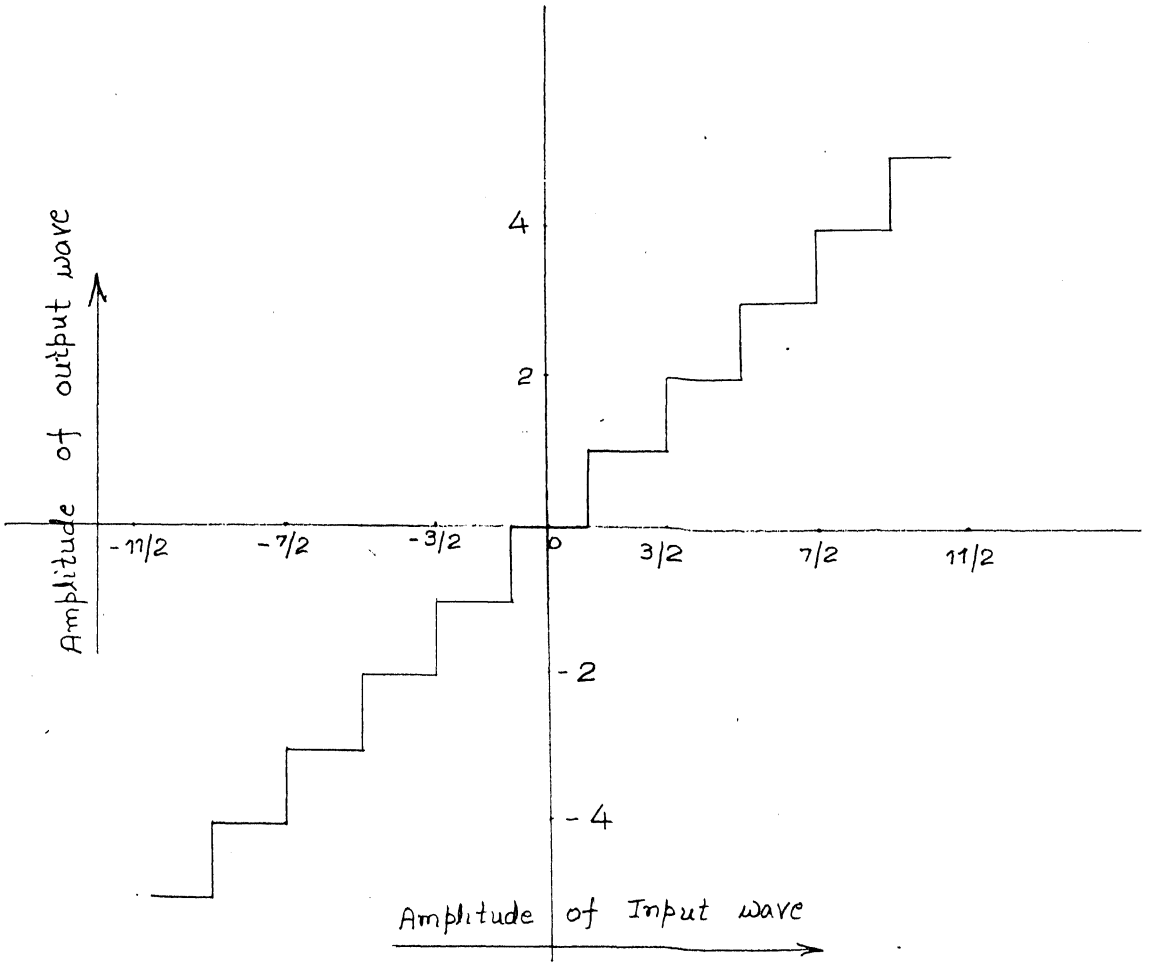

Fig. 1.2(a): Quantizing Characteristic

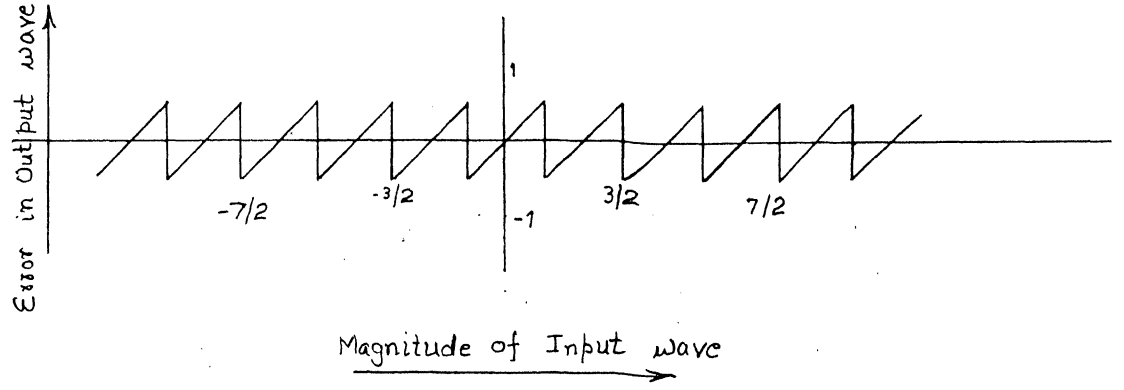

Fig. 1.2(b): Characteristics of error in quantizing

$$p(E) = \frac{1}{\Delta} , \; -\frac{\Delta}{2} \leq E \leq \frac{\Delta}{2} \qquad (1.1)$$

This will not be true if the signal overloads the quantizer as shown in Fig. 1.2.

The quantizer output might saturate at 5 for inputs exceeding that number, and the quantization error during such overload would be linearly increasing function of the input.

Assuming that the quantizer is not overloaded the mean square value if quantization noise power is

$$\int_{-\Delta/2}^{\Delta/2} E^2 \, p(E) \, dE = \frac{\Delta^2}{12} \qquad (1.2)$$

If the rms value of input X is X_{rms}, the signal to noise ratio is

$$SNR = X_{rms}^2 \; / \; (\Delta^2/12) \qquad (1.3)$$

The quality of modest complexity 32 K bits/sec PCM for a single encoding can be achieved at 24 K bits/sec but only with complex coders such as Adaptive predictive coder (APC) or Vocoder driven Adaptive transform coder (ATC). The tandem encoding performance of the more efficient codes is not as good as 64 K bits/sec PCM and significant delay is introduced by the more complex algorithms [4].

1.2 TRANSMISSION RATES IN SPEECH CODING:

Figure 1.3 shows a spectrum of speech coding transmission rates currently of interest. The figure highlights the dichotomy between nonspeech - specific waveform coders that need

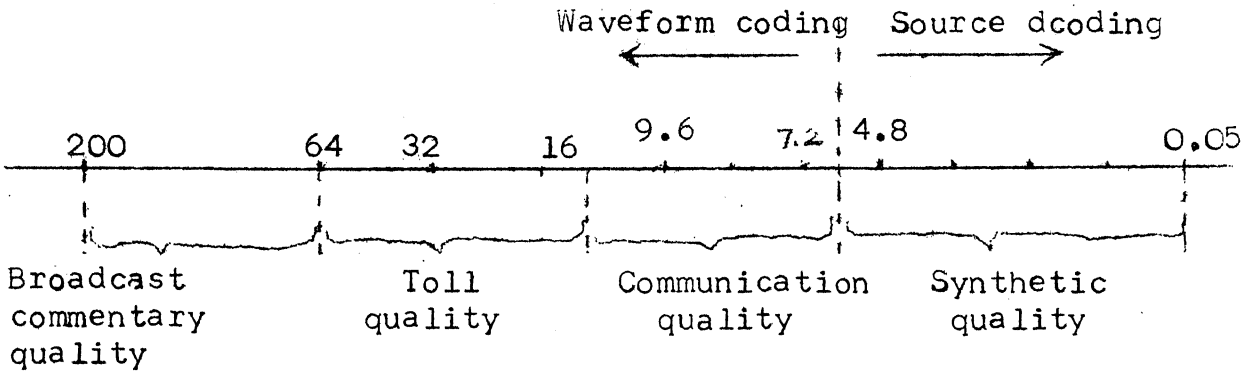

Fig. 1.3: Digital coding of speech

relatively higher transmission rates and speech specific coders for digitization at relatively lower bit rates. The figure also indicates the quality of speech reproduction that can presently be attained at a prescribed bit rate. The quality characterizations are denoted as commentary, toll, communications and synthetic [5].

The toll quality typically imply quality comparable to that of an analog speech signal having approximately the properties: (a) Frequency range = 200 to 3200 Hz, (b) signal to noise ratio $\geq$ 30 dB, (c) Harmonic distortion $\leq$ 2-3%.

At present digital coders achieve telephone toll quality for speech signals at coding rates of 16 K bits/sec and above. At bits rates exceeding 64 K bits/sec, it is possible to obtain the signal to noise ratio and harmonic distortion characteristic of toll quality with input signal bandwidths significantly wider than normal telephone (e.g. 0 to 7 KHz or better). This grade of quality is referred to as commentary quality. At rates below 16 K bits/sec and specifically the data speed range 7.2 to 9.6 K bits/sec the signal is highly intelligible, but has noticeable quality reduction, some detectable distortion and perhaps lessened talker recognition. Coders in source coding range, 4.8 K bits/sec and below, provide synthetic quality, where the signal usually has lost substantial naturalness, typically sounds reedy. Talker recognition is substantially degraded, and coder performance is talker dependent.

Perhaps the most basic property of speech waveforms is that they are band limited. The bandlimitation begins in the speech production process but an additional contribution is the finite bandwidth of typical speech transmission systems for example 200 Hz to 3200 Hz bandwidth associated with

conventional voice circuits. In any case, the finite bandwidth of speech waveform means that it can be time sampled at a finite rate (the Nyquist rate which for a low pass signal is twice the highest frequency therein; 800 Hz is a conservative sampling frequency used in commercial telephony).

CHAPTER 2

SPREAD SPECTRUM MODULATION

A spectrum, as spoken of here is a frequency domain representation of a signal. Literally a spread spectrum system is one in which the transmitted signal is spread over a wide frequency band, much wider, in fact, than the minimum bandwidth required to transmit the information being sent. A voice signal is sent with amplitude modulation in a BW only twice that of the information itself. Low deviation FM or SSB - AM also permit information to be transmitted in a bandwidth comparable to the BW of the information itself. A spread spectrum systems, on the other hand, often takes a baseband signal (voice channel) with a bandwidth of only a few KHz, and distributes it to over a wide band that may be many MHz wide. This is accomplished by modulating the information to be sent with a wide band encoding signal [6].

2.1 DEFINITION OF SPREAD SPECTRUM:

Any of a group of modulation formats in which an RF bandwidth much wider than necessary is used to transmit an information signal so that a signal to noise improvement may be gained in the process.

There are few terms explained here before getting into the details of spread spectrum.

2.1.1 Process Gain (G_p):

It is the gain or S/N improvement enjoyed by a spread spectrum system due to coherent band spreading and remapping of the desired signal. It is expressed by the equation

$$G_p = \frac{(BW)_{RF}}{R_{info}} = TW \qquad (2.1)$$

where the RF bandwidth $(BW)_{RF}$ is the bandwidth of the transmitted spread spectrum signal and the information rate (R_{info}) is the data rate in the information base band channel.

2.1.2 TW (TW product):

It is the equivalent of G_p or process gain where T is the period of information sent and W is the bandwidth employed to send it that is $T = 1/R_{info}$.

2.1.3 Jamming Margin:

Jamming margin expresses the capability of a system to perform in a hostile environment when faced with interfering signal having a power level larger than the desired signal by the amount of the available process gain. Jamming margin

takes into account the requirement for a useful system output signal to noise ratio and allows for internal losses; that is:

$$\text{Jamming margin: } G_p - [L_{SYS} + (\frac{S}{N})_{OUT}]$$

where L_{SYS} = system implementation losses

$(\frac{S}{N})_{OUT}$ = signal to noise at the information output.

2.2 PSEUDO NOISE:

It is a term used to signify any of a group of code sequences that exhibit noise like properties. Also sometimes used as a name for systems that employ pseudo noise code modulation.

Spread spectrum techniques are of interest in which some signal or operation other than information being sent is used for spreading the transmitted signal.

There are three general types of modulation in the spread spectrum system:

a) Direct sequence modulated system: In this process the carrier is modulated by a digital code sequence whose bit rate is much higher than the information signal bandwidth.

b) Frequency hoppers: In this system the carrier frequency is shifted in discrete increments in a pattern dictated by a

a code sequence, which are called, frequency hoppers. The transmitter jumps from one frequency to any other within some predetermined set; the order of frequency usage is determined by a code sequence.

c) Pulsed FM or 'chirp' modulation in which a carrier is swept over a wide band during a given pulse interval.

Closely akin to the frequency hoppers are time hopping and time frequency hopping systems whose chief distinguishing feature is that their time of transmission (usually a low duty cycle and short duration) is governed by a code sequence. In time frequency hoppers, it follows that the code sequence determines both the transmitted frequency and the time of transmission.

The basis of spread spectrum technology is expressed by Shannon in the form of channel capacity

$$C = W \log_2 (1 + \frac{S}{N}) \qquad (2.2)$$

where C is capacity in bits per second

W is bandwidth in hertz

S is signal power

N is noise power

This equation shows the relationship between the ability of a channel to transfer error free information

compared with S/N existing in the channel and the BW used to transmit the information. Letting C be the desired system information rate and changing bases we find

$$\frac{C}{W} = 1.44 \log_e \left(1 + \frac{S}{N}\right)$$

and for S/N small say ≤ 0.1

$$\frac{C}{W} = 1.44 \frac{S}{N} \qquad (2.3)$$

since $\log_e \left(1 + \frac{S}{N}\right) = \frac{S}{N} - \frac{1}{2}\left(\frac{S}{N}\right)^2 + \frac{1}{3}\left(\frac{S}{N}\right)^3 - \frac{1}{4}\left(\frac{S}{N}\right)^4 \ldots$

$-1 < \frac{S}{N} < 1$ by the logarithmic expansion

from this equation we find

$$\frac{N}{S} = \frac{1.44W}{C} \backsimeq \frac{W}{C}$$

$$W = \frac{NC}{S} \qquad (2.4)$$

We see that for any given noise to signal ratio we can have a low information error rate by increasing the bandwidth used to transfer the information; for example if we want a system to operate in a link in which the interfering noise is 100 times greater than the signal and our information rate is 3 Kilobits per second then our 3 K bits/sec information must be transmitted with a bandwidth of

$$W = \frac{NC}{S \times 1.44} = \frac{100}{1} \times \frac{3 \times 1000}{1.44}$$

$$W = 2.08 \times 10^5 \text{ Hz} \simeq 208 \text{ Khz}$$

Incidentally the information itself may be embedded in the spread spectrum signal by several methods. The most common is that of adding the information to the spectrum spreading code before its use for spreading modulation.

A spread spectrum must meet two criteria:

(a) The transmitted B.W. is much greater than the B.W. or rate of the information being sent.

(b) Some function other than the information being sent is employed to determine the resulting modulated RF bandwidth.

Essence of spread spectrum communications

i) Expanding the B.W. of a signal.

ii) Transmitting the expanded signal.

iii) Recovering the desired signal by remapping the received spread spectrum into the original information bandwidth.

In the process of carrying out this series of bandwidth trade off, the purpose is to allow the system to deliver error free information in a noisy signal environment. While

sacrificing linear channel bandwidth and increasing system complexity, spread spectrum techniques permit low probability of intercept and jam resistant communication. Additional attributes of spread spectrum communications include multiplexing efficiency in a nonlinear channel, selective calling, identification, multipath protection and accurate time of arrival measurement. Use of spread spectrum is not limited to communication systems but navigation, identification and radar system also currently benefit from spectrum spreading.

2.2.1 Pseudo Random Sequences:

To say that a finite sequence of numbers, or digits, or events of any sort is random, is strictly speaking, a comment on the manner in which the sequence was generated, rather than on the actual terms which appear in the sequence. That is, a process such as coin flipping, which selects objects from a 'sample space' in an unpredictable fashion, but in accordance with some probability distribution, is a random process. Hence randomness refers to the a priori circumstances of sequence generation. Given a list of tests for the plausibility of randomness, we may define any sequence which passes the test to be pseudo random. One of the simplest and most effective devices for generating deterministic sequences of ONE's and ZERO's for such purposes as digital

communications is the shift register. Moreover, there is an important class of rather simple shift register which generate sequences that pass several of the most obvious randomness tests.

Hence PN sequences are repeatable sequences consisting of a semirandom distribution of 1's and 0's. Otherwise if their binary distribution is completely random, the sequence would be non-deterministic and therefore unusable in any application requiring synchronous sequences.

2.3 SHIFT REGISTER SEQUENCES:

A shift register of degree n is a device consisting of n consecutive binary storage positions, which shifts the contents of each position to the next position down the line, in time to the regular beat of a clock (or other timing device). In order to prevent the shift register from employing by the end of n clock pulses, a feedback term may be computed as a logical function of the contents of the n positions and fed back into the first position of the shift register. The general block diagram of such a shift register with feedback is shown in Fig. 2.1 [7].

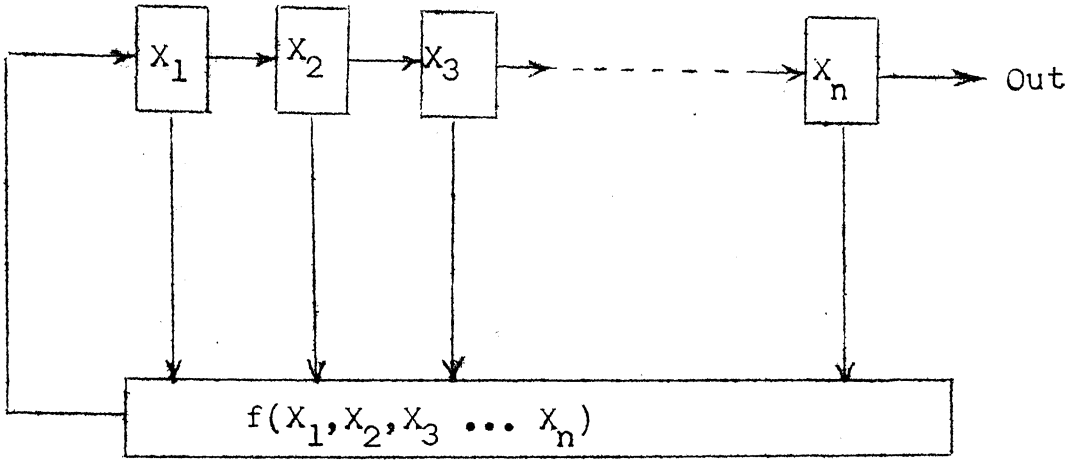

Fig. 2.1: Scheme for shift register sequence of degree n

For the shift register sequence as shown in the diagram, the output sequence is always ultimately periodic, with a period p not exceeding 2^n. If the shift register is linear, the period is at most 2^n-1, and any output sequence achieving $p = 2^n-1$ is called a maximum length linear shift register sequence.

For every n, there exist maximum length linear shift register sequences and these are all pseudo random in the sense that they satisfy the following three 'randomness properties'.

i) The Balance Property: In each period of the sequence the number of ONE's differs from the number of ZERO's by at most 1.

ii) The Run Property: Among the runs of ONE's and of ZERO's in each period, one-half the runs of each kind are of length one, one-fourth of each kind are of length two, one-eighth are of length three, and so on as long as these fractions give meaningful numbers of runs.

iii) The Correlation Property: If a period of the sequence is compared, term by term, with any cyclic shift of itself, the number of agreements differs from the number of disagreements by at most 1.

Maximal length sequences are a particular class of PN sequences, They are typically generated by modulo 2 summation and feedback of selected outputs of shift register (as shown in Fig. 2.2).

When produced by a shift register of length n, maximum length sequences have a period of 2^{n-1} bits. The total number

of 1's in a maximal length sequence is exactly one greater than the total number of zeros.

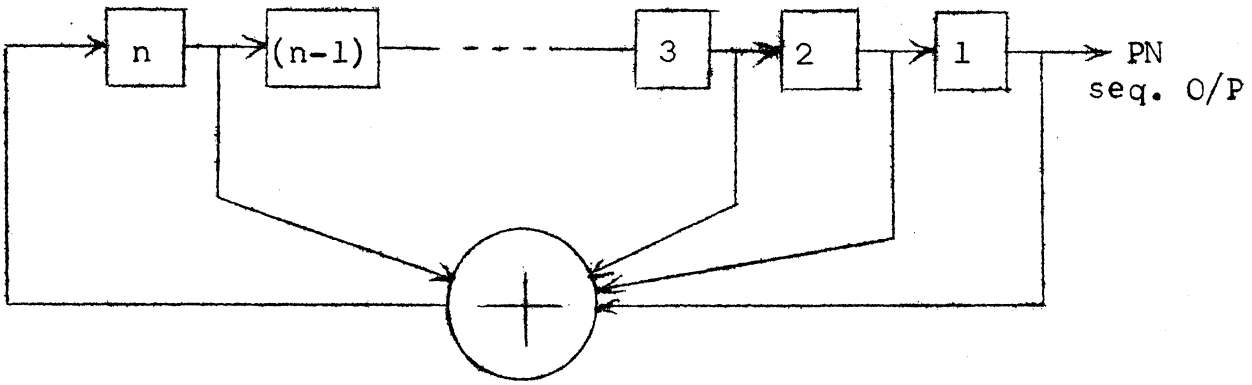

Fig. 2.2: Generalised shift register PN sequence generator.

2.3.1 Application of Shift Register Sequences:

The ideas of using shift register to generate sequences of ONE's and ZERO's has been explored, developed and refined in the past. It is the purpose here to list and briefly describe what the principal areas of application are. Moreover some of other properties of shift register sequences which make them well suited to these various applications are indicated. The discussion is supplementary to the main theme of the thesis and is included in order to indicate the broad range of applications.

i) Secure and Limited-Access Code Generators: A message written in binary digits could be added, modulo 2, to a shift register acting as the 'Key'. The deciphering consists of adding the key modulo 2 to the coded message. This type of cipher is only one of many classical encipherments in which a shift register sequence could play the role of the key.

ii) Privacy Encoding: There are many situations where one wishes to communicate a message (most typically a command) through a hostile environment where the information need not remain secret after it is received and has been acted upon. There the use of shift register sequences to provide positive authentication of the message is an attractive possibility.

iii) Multiple Address Coding: Different portions of a long shift register sequence can be assigned as characteristic addresses to a large number of individuals, aircrafts, sub-stations, etc. These addresses may be used either for positive identification, or merely to enable a large number of scattered messengers to report systematically to their home base.

iv) Efficiency Code Generator: A remarkable assortment of schemes for error-correcting codes based on linear shift register sequences have been proposed and studied.

v) Signals Recoverable through Noise: For range radar applications in environments with extreme background noise, a shift register modulated pulse train or CW signal, using a maximum length sequence, has the property that its auto-correlation function is recoverable despite a noise-to-signal excess of many decibels.

vi) Prescribed Property Generator: It has been proved that with a shift register of degree n, all sequence lengths p between 1 and 2^n (inclusive) can be obtained by use of a suitably chosen feedback logic. A typical application is to the construction of a 'count down' circuit within a synchronous digital system.

2.4 SPREAD SPECTRUM DIGITAL COMMUNICATION SYSTEM:

The block diagram shown in Fig. 2.3 illustrates the basic elements of a spread spectrum digital communication systems with a binary information sequence at its input at the transmitting end and at its output at the receiving end. In addition to these elements, there are two identical pseudo random pattern generators, one which interfaces with the modulator at the transmitting end and the second which interfaces with the demodulator at the receiving end. The generators generate a pseudo random or pseudo noise (PN) binary

valued sequence which is impressed on the transmitted signal at the modulator and removed from the received signal at the demodulator.

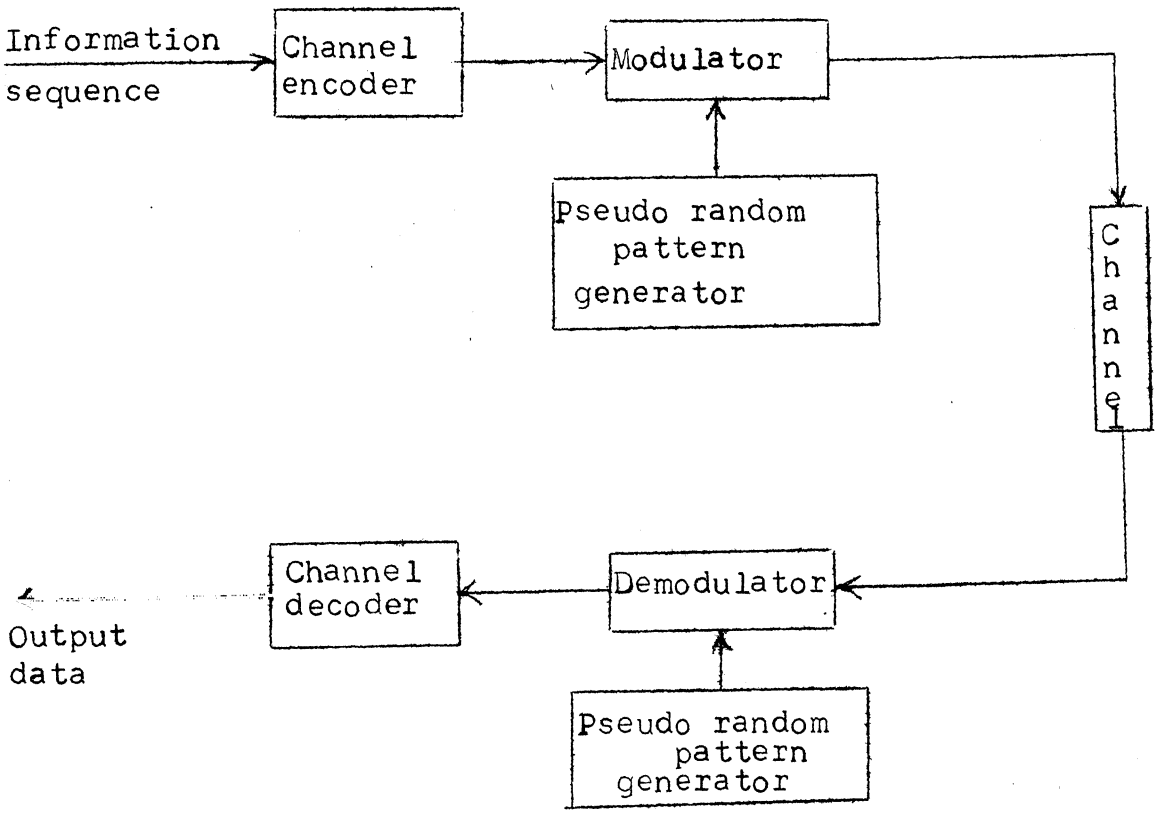

Fig. 2.3: Block diagram of spread spectrum digital communication system.

Synchronization of the PN sequence generated at the receiver with the PN sequence contained in the incoming received signal is required in order to demodulate the received signal. Initially, prior to the transmission of information, synchronization may be achieved by transmitting a fixed pseudo-random bit pattern which the receiver will recognize in the presence of interference with a high probability. After time synchronization of the generators is established, the transmission of information may commence.

CHAPTER 3

SPREAD SPECTRUM TRANSMITTER

3.1 SYSTEM SPECIFICATIONS:

Input signal : (0-10) volts (peak to peak), (0-4) KHz signal.

Transmitter frequency : 1 MHz (direct sequence modulated output)

Sampling rate: 8.33 KHz

Waveform coding: 66.66 KHz PCM

Noise to signal ratio : 30 dB

Jamming margin : 18 dB

The system works for single audio channel with the interfering noise 1000 times greater than signal and jamming margin of 18 dB. The direct sequence modulated spread spectrum transmitter works on 1 MHz frequency so that it may be directly interfaced with 1 MHz operating system moreover this frequency range provides ease for selection of hardware components. The block diagram of system implementation is as follows. The specifications meet the requirement of the user.

3.2 SYSTEM IMPLEMENTATION:

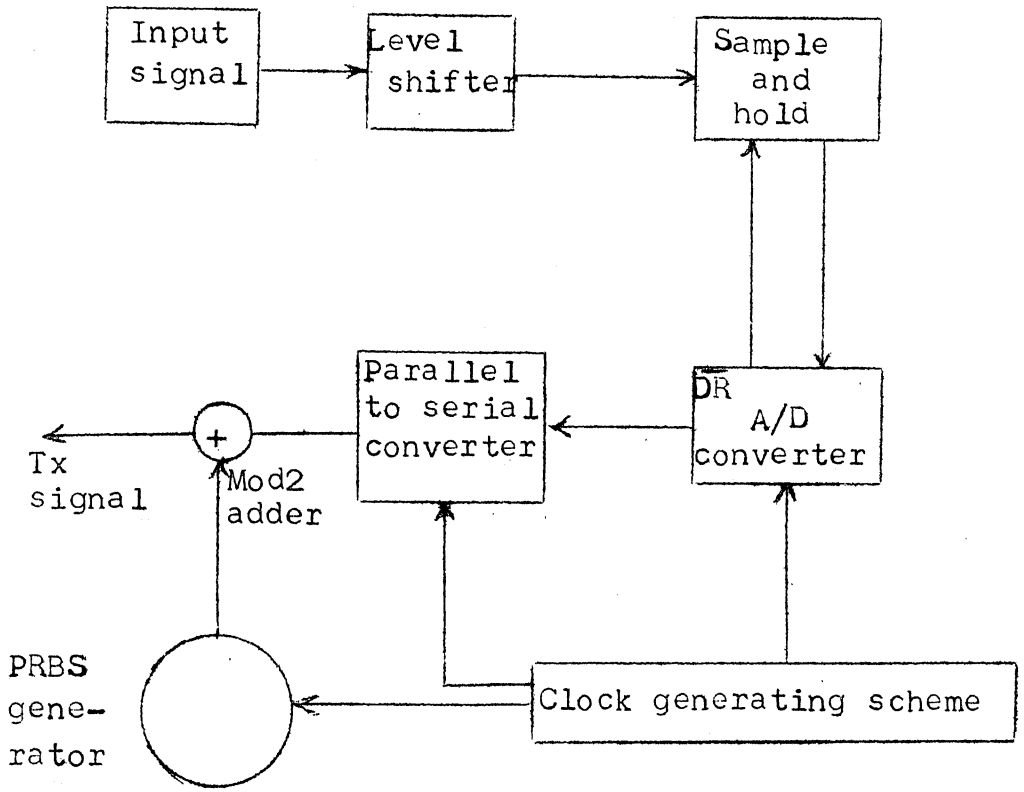

Fig. 3.1: Block diagram of transmitter

The block diagram of all the stages of the transmitter is shown in Fig. 3.1. The input signal is taken from audio oscillator which simulates the speech signal. The second block is level shifter which is designed using operational amplifiers, it provides isolation and protects further stages against any spurious input signals. The level shifter also provides the d.c. shift to input signal

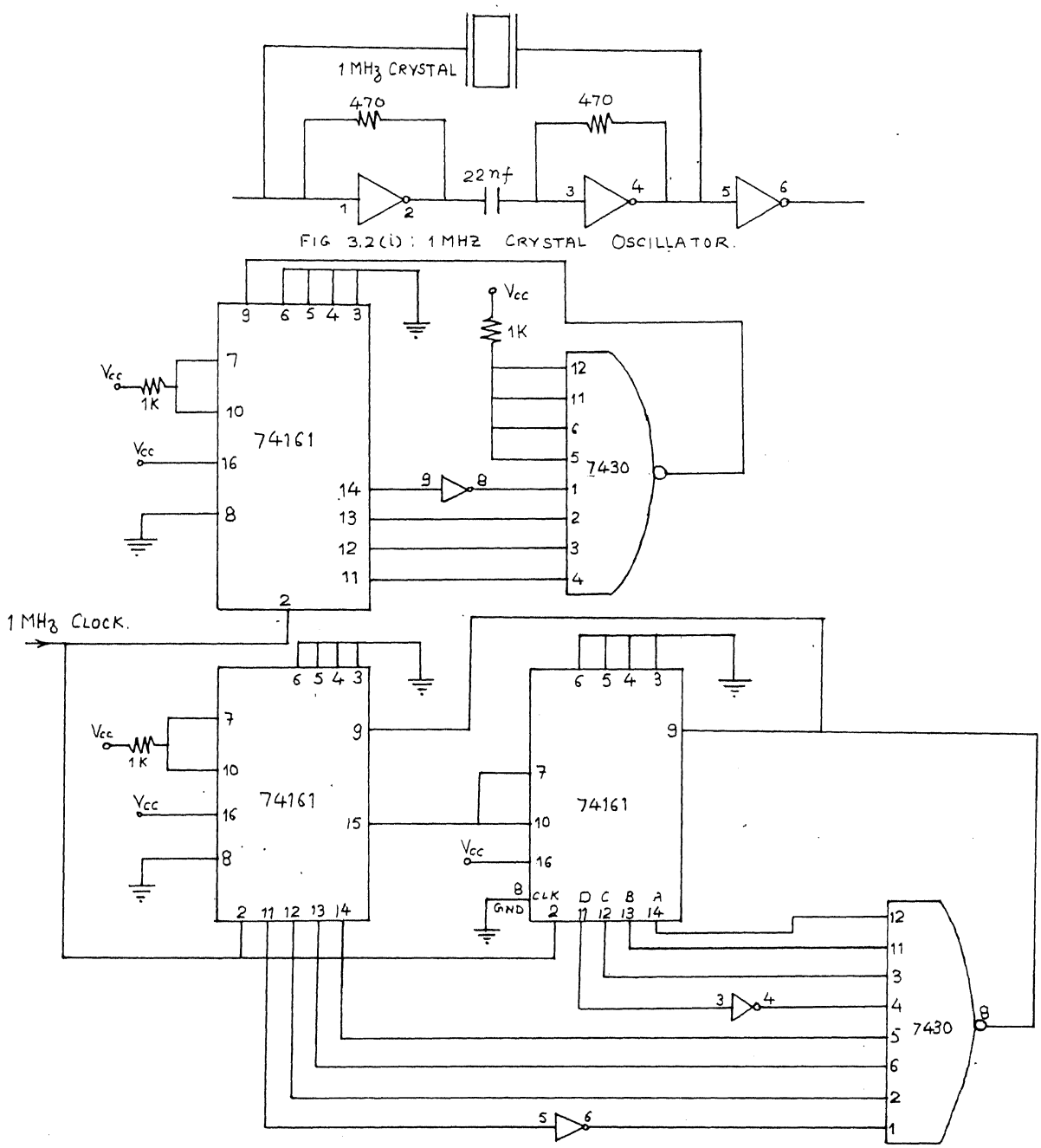

FIG 3.2(i) : 1 MHZ CRYSTAL OSCILLATOR.

Fig. 3.2(ii) 8.33 KHz and 66.66 KHz frequency divider circuits

in accordance with the input voltage limits of the analog to digital converter. The sample and hold circuit gets the clock from $\overline{\text{DATA READY}}$ line of A/D converter.

The analog to digital converter gets 8.33 KHz clock to convert the input signal to the 8 bit digital information. The pulse code modulated output is achieved by passing the digital information through the parallel to serial converter. At this stage, the synchronization bit is added to the signal for the frame synchronization in the receiver. A four bit shift register is used for the generation of 15 bit PN sequence. This PN sequence EX ORed with PCM output provides the spread spectrum modulated 1 MHz signal at the output of the transmitter. The details of the subsystems are described below.

3.3 CLOCK GENERATING SCHEME:

The circuit shown in Fig. 3.2(i) provides basic 1 MHz clock for the spread spectrum modulator circuitry. The capacitor can be fixed to any value for clock generation but for 1 MHz clock its value is found to be 22 nf. As this 1 MHz clock is used for frequency division and spread spectrum clock, there is chance of overloading the pin 4 of inverter and hence another inverter is connected at the output stage of this circuitry which acts as buffer and protects 1 MHz clock from overloading.

For deriving 8.33 KHz clock for analog to digital converter and 66.66 KHz for PCM scheme, the counter feedback logic is implemented. As shown in Fig. 3.2(ii), a 74161 four bit binary counter with asynchronous clear and 8 input NAND gate is used with some inverter logic to decode the proper output stage. In 66.66 KHz clock generation, enable points of counter are tied high and load pin is fed back from decoder logic which decodes the fifteenth clock pulse and generates a low level pulse for loading again zero at the counter output pins (as the load inputs are connected to zero logic state). Hence this counter counts only upto fifteen and acts as divide by fifteen counter. The pin 11 of counter provides the 66.66 KHz clock output.

The 8.33 KHz clock for A/D converter is achieved using the similar logic with two 4 bit binary counters (74161). In this divider circuitry, first counter is permanantly enabled and its ripple carry output is connected to enable inputs of second counter. So that in the open loop system i.e. without feedback logic for load inputs the second counter works as divide by 256 counter. Now similar to the previous counter divider, the count of 120 (15x8) is decoded by 8 input NAND gate with some additional inverter logic. The output of decoder circuit is connected to the load pins of both the

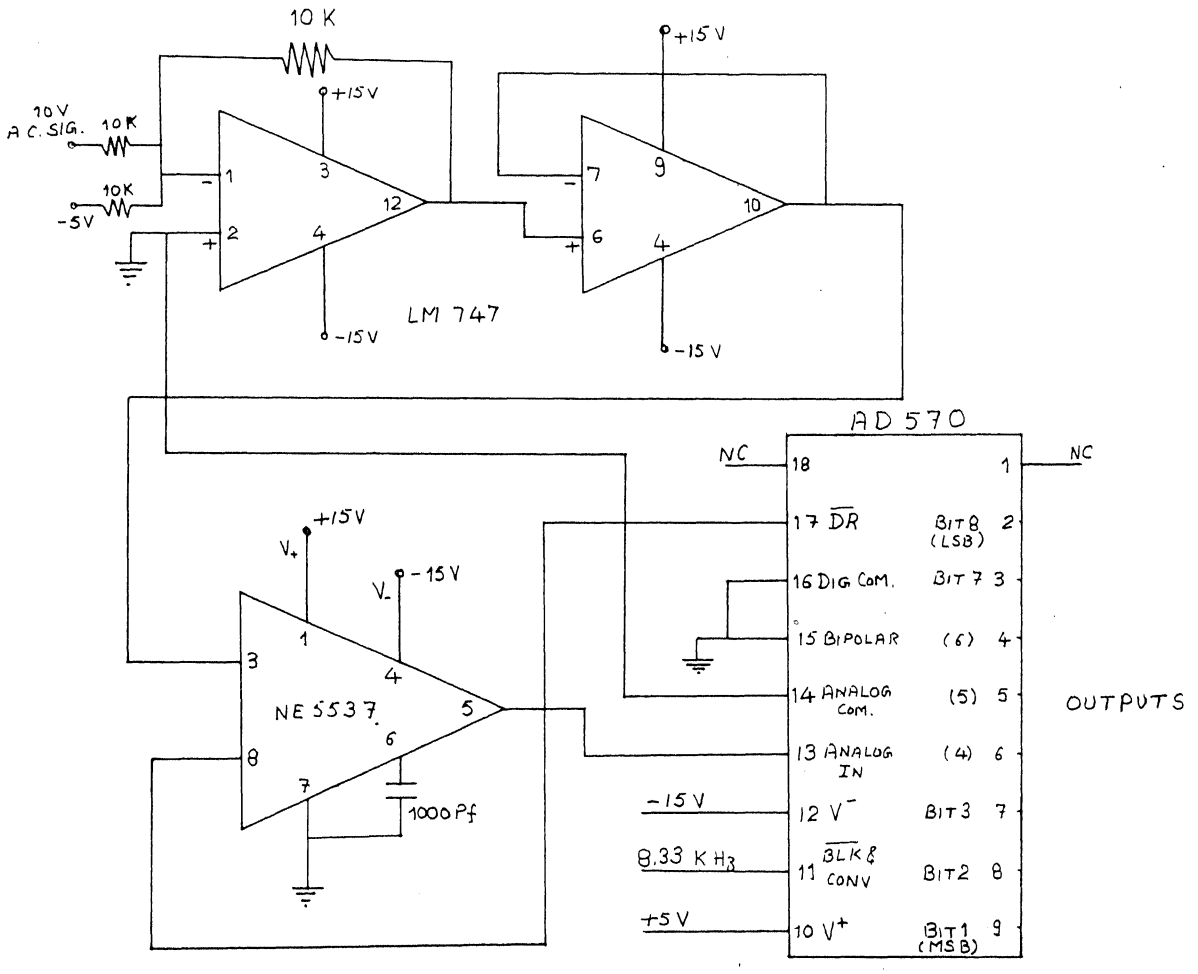

Fig. 3.3: Level shifter, sample and hold and A/D Converter

counters. All the load inputs of both thecounters are connected to zero state so with this feedback logic this circuit works as divide by 120 counter and provides the desired 8.33 KHz clock. Both the frequency division schemes are developed separately so that delay of one counter circuitry is not reflected to other.

3.4 LEVEL SHIFTER, SAMPLE AND HOLD AND A/D CONVERSION:

In the present work the speech signal is simulated by an audio oscillator and as the complete range of analog to digital converter is zero to ten volts, the output of audio oscillator is fed to operational amplifier circuitry to provide signal in proper range.

In the first stage of operational amplifier, the audio oscillator output and a d.c. shift level are provided as inputs, this stage provides a d.c. shift to the input signal so that analog output varies from zero to ten volts. Next is the source follower stage to protect the next stages of transmitter. Hence the opamp circuitry provides a d.c. level shift and a buffer stage which improves the driving capacity of input signal as well as isolates the transmitter circuitry from any external spurious signal.

After the operational amplifier stage, an 8 bit analog to digital converter and a sample and hold device is used. In the present circuitry as shown in Fig. 3.3, 8 bit successive approximation AD 570 analog to digital converter is used which operates on +5 volts and -15 volts power supplies. The AD570 accepts analog inputs zero to +10 volts or bipolar ±5 volts, externally selectable. As the blank and $\overline{\text{convert}}$ input is driven low, the three state outputs will be opened and a conversion will commence. Upon the completion of the conversion the $\overline{\text{data ready}}$ line will go low and data will appear at the output. Pulling the blank and $\overline{\text{convert}}$ input high blanks the outputs and readies the device for next conversion. The AD 570 executes a true 8 bit conversion with no missing codes in approx. 25 μs.

The A/D 570 accepts either a unipolar (0 to +10 volts) or bipolar (-5 volts to +5 volts) analog inputs by simply grounding and opening a single pin. In the present circuit it is used in zero to +10 volts mode by shorting pins 15 and 16 and connecting the analog input at pin 13. The operation is guaranteed with -15 volts and +5 volts power supplies but the device will also operate with -12 volts supply.

For standard operation after connecting the power supplies only the conversion start pulse is required. The

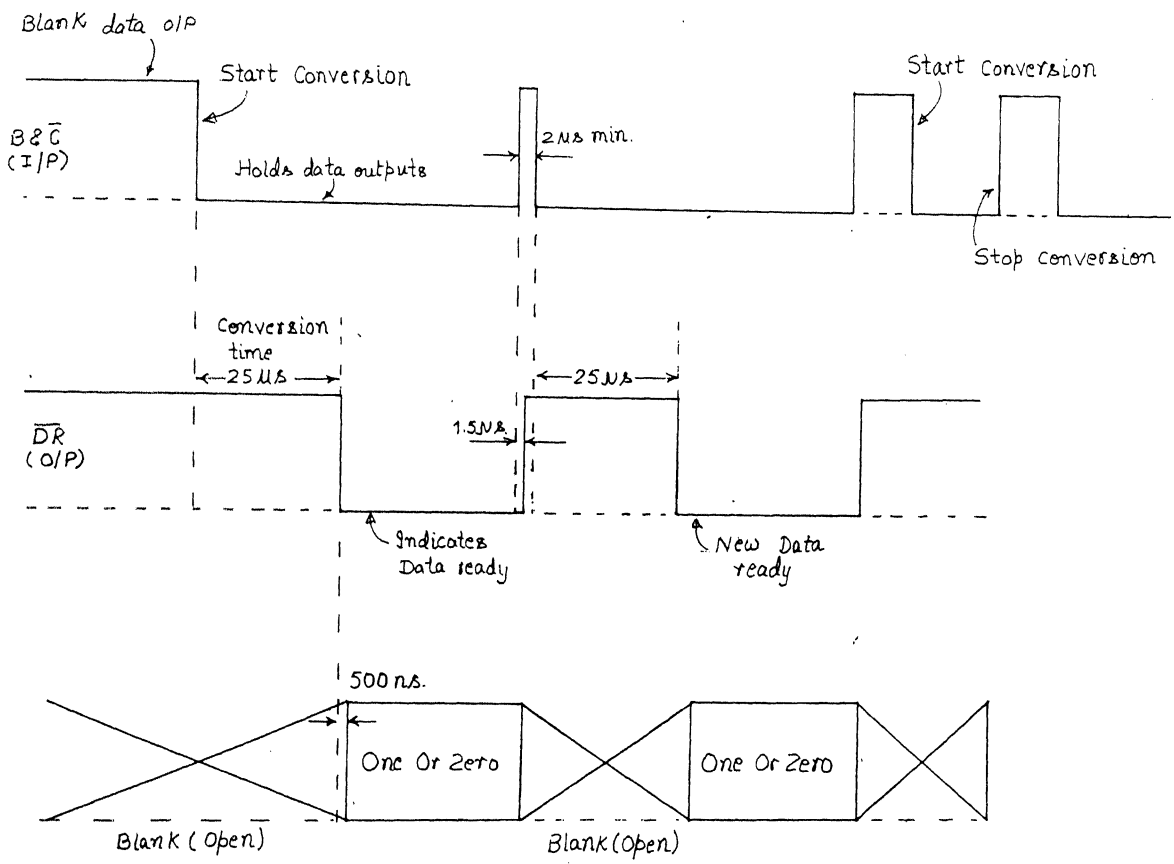

Fig. 3.4: Timing Diagram of AD570

nominal 9.961 volts full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to pin 14. If a more precision calibration is desired a 200 Ω trimmer should be used instead.

3.4.1 Bipolar Operation:

The standard unipolar operation zero to +10 volts is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5 volts to +5 volts range with an offset binary code (-5.00 volts in will give a 8 bit code of 0000 0000, an input of 0.00 volt results in an output code of 1000 0000 and 4.96 volts at the input yields the 1111 1111 code).

3.4.2 Control of Timing of AD 570:

The normal standby situation is Blank and $\overline{\text{convert}}$ (B and $\overline{C}$) line is held high, the output lines will be 'open' and the $\overline{\text{Data Ready}}$ (output) line will be high, this mode is the lowest power state. When (B and $\overline{C}$) line is brought low, the conversion cycle is initiated; but the $\overline{DR}$ and data line do not change states. When the conversion cycle is complete (typically 25 μsec), the $\overline{DR}$ line goes low and within 500 ns, the data lines become active with the new data.

About 1.5 μsec after the blank and $\overline{\text{convert}}$ line is again brought to high, the $\overline{\text{Data Ready}}$ line will go high and the data lines will go open. When the Blank and $\overline{\text{convert}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the blank and $\overline{\text{convert}}$ line to blank previous data and start a new conversion is 2 μsec. If the blank and $\overline{\text{convert}}$ line is brought high during a conversion, the conversion will stop and the $\overline{\text{Data Ready}}$ and data lines will not change. If a 2 μsec or longer pulse is applied to the B and $\overline{C}$ line during a conversion, the converter will clear and start a new conversion cycle. All these timing sequences are shown in Fig. 3.4. As the B and $\overline{C}$ gets 8.33 KHz signal, this A/D converter meets all the timing requirements of the present circuitry.

3.4.3 Sample and Hold Amplifier:

NE 5537 is used for its fast acquisition time and low droop rate, as shown in Fig. 3.3. The two operational amplifiers as shown in Fig. 3.5, function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistor which gives the system a low offset voltage. The second amplifier has JFET input transistor to achieve low leakage current. The output stage has the capacity to drive a 2K Ω load.

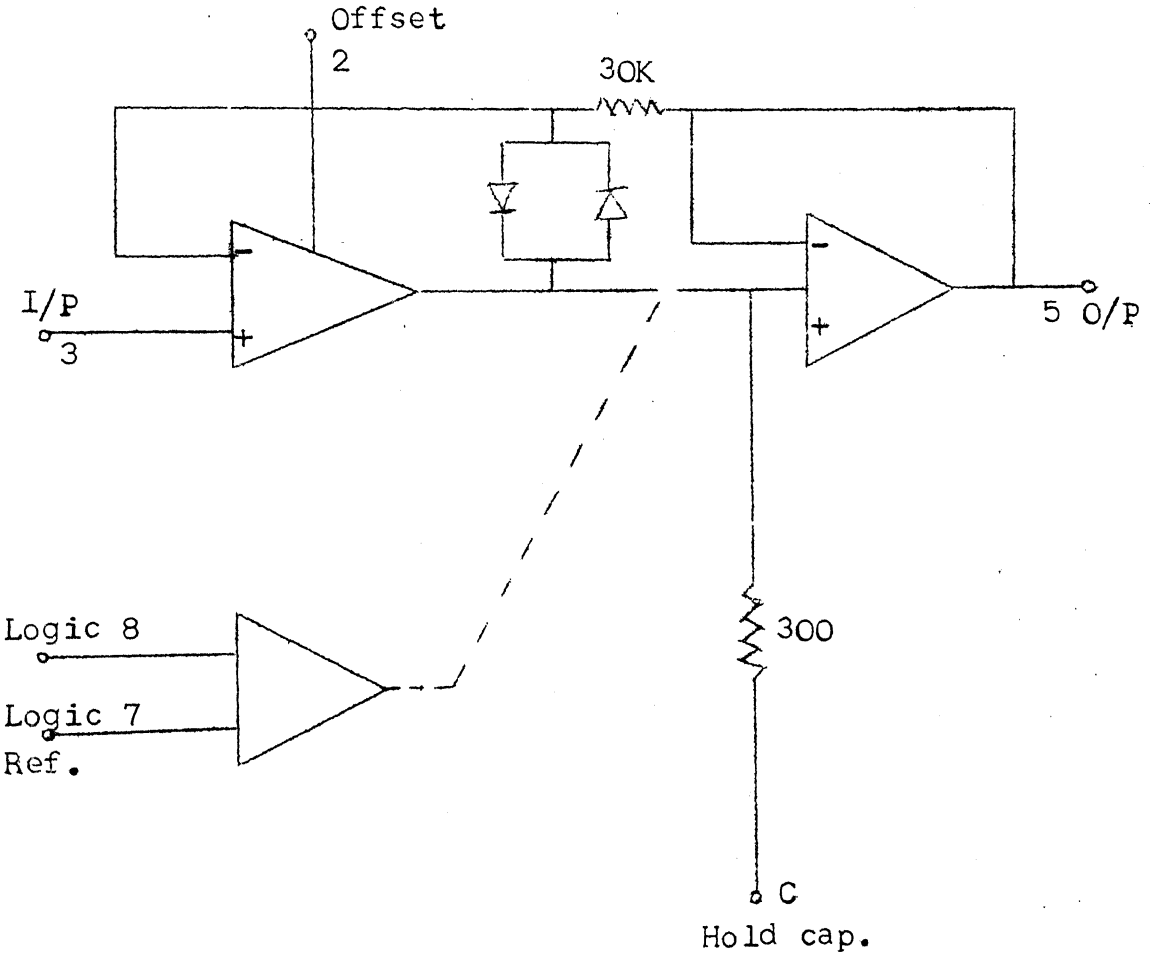

Fig. 3.5: Sample and Hold Amplifier

The principle application for sample/track hold amplifier is to maintain an analog to digital converter's input constant during conversion, at a value representing analog input as of a certain precisely known time. The characteristics of sample and hold amplifier are crucial for system accuracy

and the reliability of digital data, especially in 12 bit and/or high throughput rate applications.

A sample/track hold amplifier as its name indicates, has two modes of operations, programmed by a digital control input. In the track or sample mode, the output follows the input, usually with a gain of +1 when the mode input switches to hold, the output of sample and hold amplifier ideally retains the last value it had when the command to hold was given and it retains that value until the logic input dictates (track) sample, at which time the output ideally jumps to the input value and follows the input until the next hold command is given.

3.4.4 Circuit and Hardware:

A sample hold amplifier usually consists of a storage capacitor, input and output buffer amplifiers and a switch and its drive circuitry. During sample, the circuit is connected to promote rapid charging of a capacitor. During hold, the capacitor is disconnected from its charging source and ideally retains its charge.

During the sample to hold, hold and hold to sample states, the dynamic nature of mode switching introduces a number of specifications that are particular to sample and hold

amplifiers. The most important are aperture time and its uncertainty, sample to hold step and acquisition time.

Acquisition time is the time required by the output of the device to reach its final value within a specified error band, after the sample command has been given. Included are switch delay time, the slewing interval and settling time for a specified output voltage change. Aperture (delay) time is the time required after the hold command to open fully. The sample is, in effect, delayed by this interval, and hold command would have to be advanced by this amount for precise timing.

The differential logic threshold is 1.4 volts with the sample mode occuring when the logic input is high. For proper logic operations, however, one of the logic pins must always be at least 2 volts below the positive supply and 3 volts above the negative supply. As shown in Figure $\pm$15 volts is used as power supplies. The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. The switch control has a floating reference (pin 7) referred to as logic reference which makes the sample and hold device compatiable to several types external logic signals. The switching device operates

at a threshold level of 1.4 volts. As shown in Fig. 3.3, the logic input is connected to $\overline{DR}$ of A/D converter. Sampling time for NE 5537 is less than 10 μsec (measured to 0.1% of input signal), leakage current is 6 PA at a rated O/P load of 2KΩ. The aperture time of the device is 4 μsec for C_n equals to 1000 pf. The operational amplifier circuit output is connected to input pin 3 of sample and hold device and its output pin 5 goes to pin 13 of A/D converter. The A/D converter gets 8.33 KHz clock at Blank and $\overline{convert}$ from clock generating block. This part of the circuit consists of digital and analog ground and hence special care is taken for grounding. The digital and analog grounds are common only at the power supply end. The A/D converter has got both analog and digital ground while sample and hold gets analog ground only.

3.5 PARALLEL TO SERIAL CONVERTER:

The parallel to serial converter circuit consists of two 4 bit bidirectional universal shift register (74194), a D flip flop (7474) and a dual retriggerable monostable multivibrator with clear (74123). The basic operation is done by shift registers. It contains 46 gates and features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs and a direct over-riding clear line.

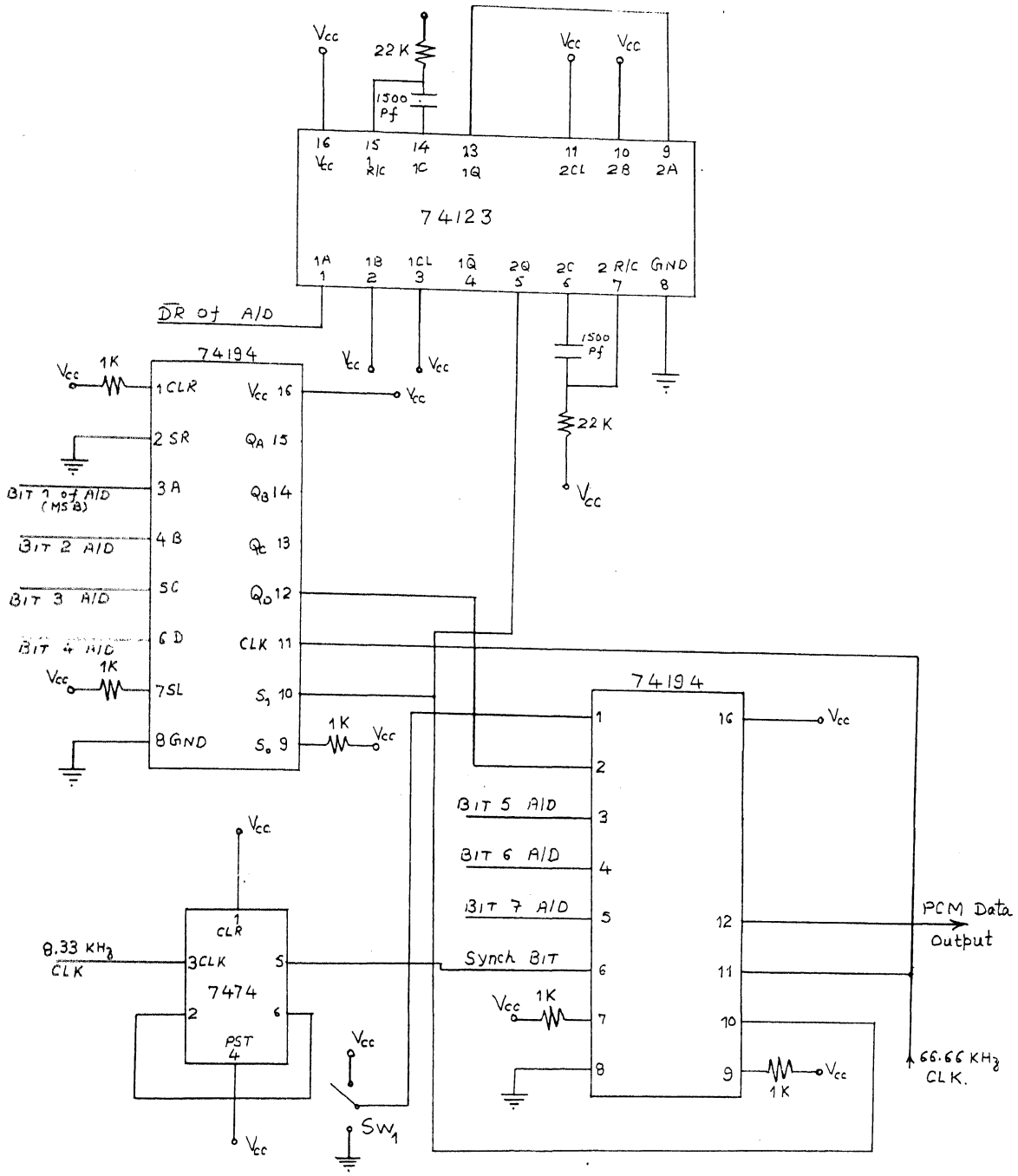

Fig. 3.6: Parallel to Serial Converter

This register has four distinct modes of operation namely:

parallel (broad side) line
shift right (in the direction Q_A towards Q_D)
shift left (in the direction Q_D towards Q_A)
inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs S_0 and S_1 high. The data are loaded into the associated flip flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking of the flip flop is inhibited when both mode control inputs are low. The mode controls of the 74194 should be changed only while the clock input is high.

Now as shown in Fig. 3.6, two shift registers are connected in series for 8 bits of digital data from A/D output. The last output pin of first shift register is

connected to shift right serial input of second shift register. The first four maximum significant bits of analog to digital converter are connected to first shift register and rest of the three bits are connected to A,B and C inputs of second shift register. In this scheme a D flip flop is used for adding synch. bit at PCM data output. The D flip flop acts as frequency divider and gets 8.33 KHz clock as input, its output is connected to pin 6 of second shift register. So this flip flop creates an alternate sequence of one's and zero's in 8 bit length of stream at the output of second shift register. This synch. bit is used for frame synchronization in receiver circuitry. The shift registers get 66.66 KHz at clock inputs and so is kept permanantly high because the shift registers are used in shift right and loading modes only. Now whenever S_1 is low the data is shifted right and when it is high, data is loaded from input pins. The clear pin of first shift register is kept high and the clear pin of second shift register is taken out and connected to a switch. This switch is used for suppressing the data, whenever clear pin is low the data is suppressed otherwise data is allowed. This feature is useful for pseudo random bit synchronization in the receiver. As the shift left serial input feature is not used in this particular configuration, the pin 7 of both the shift registers are kept

high. The $\overline{DR}$ line of AD 570 is taken to dual retriggerable monostable multivibrator. The output of monostable is connected to pin S_1 of the shift registers. The monostable ensures that data is changed at the rising edge of the clock. Now at the output of the shift registers the flow of data is from MSB to LSB and every 8th bit is synch. bit.

In 74123 both the monostables are used which provide a delay of 20 μsec and its output is fed to pin S_1 of shift registers. The pulse width calculation is done by the following formula

for C_{ext} > 1000 pf

$$t_\omega = K R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right), \quad K = 0.28 \text{ for } 74123$$

where R_T is in KΩ, C_{ext} in pf, t_ω in nano seconds

for t_ω = 10 μsec

$$10000 = 0.28 R_T \times 1500, \left(1 + \frac{0.7}{R_T}\right)$$

$$= 28 \times 15 \, (R_T + 0.7)$$

R_T = 24.3KΩ for C_{ext} = 1500 pf.

3.6 SPREAD SPECTRUM MODULATOR:

The PN sequence described in the previous part is used as shown in Fig. 3.7. The NOR gate is used so that the sequence is made self starting. If this NOR gate is not provided,

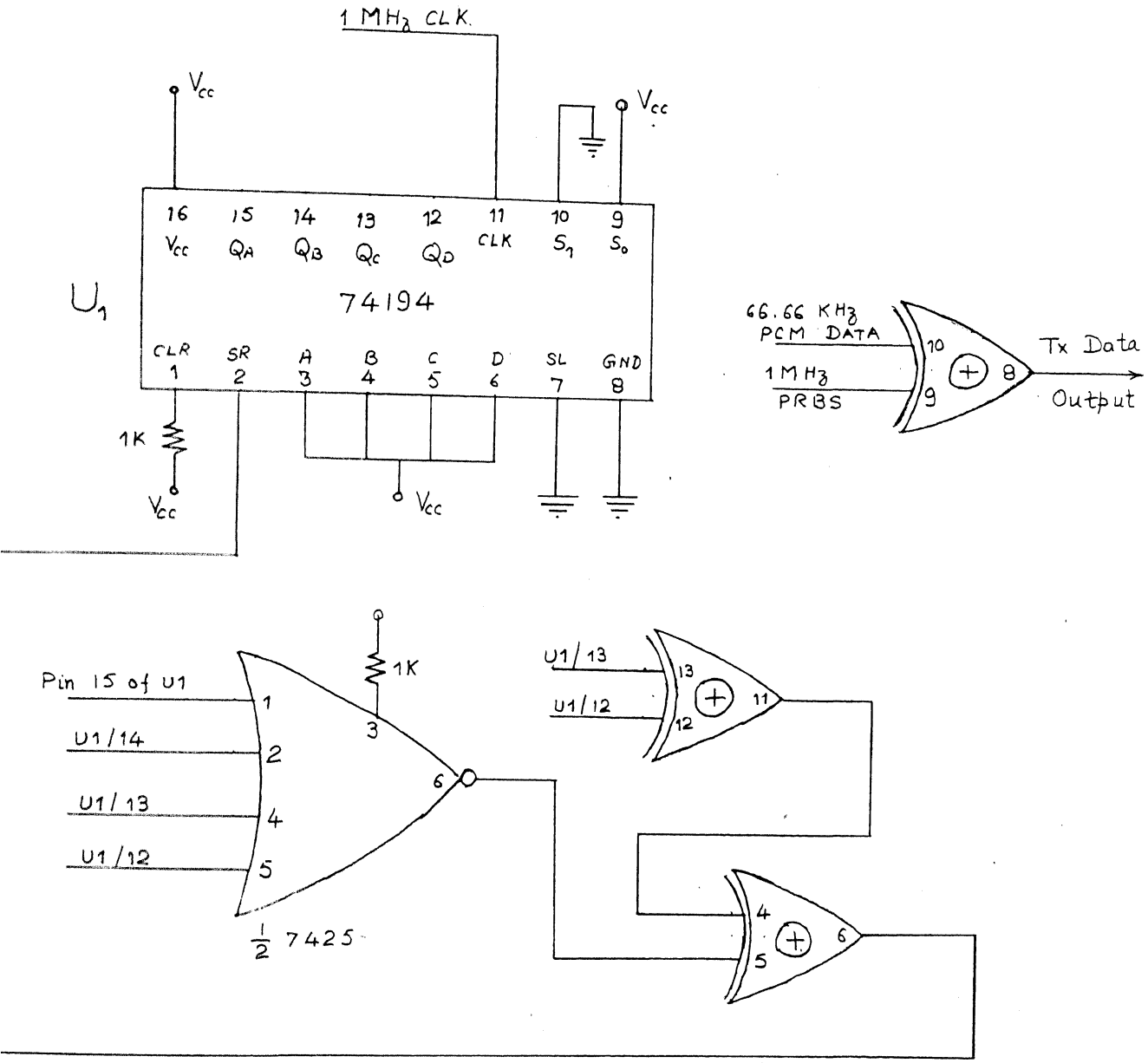

Fig. 3.7: Spread Spectrum Modulator

the PN sequence won't follow for all zero state. The shift register gets 1 MHz clock and all load inputs are kept high. To make this shift register to work in shift right mode, S_0 is connected to V_{CC} and S_1 is kept low. Two EX-OR gates are used for feedback logic. First EX-OR gets pin 12 and pin 13 of U1 (Q_C and Q_D of 74194) as inputs, the output of this EX-OR and the output of NOR is again exclusive ored for the shift right serial input connection of the shift register. Now this circuit works as 15 bit pseudo random sequence generator. This 1 MHz 15 bit pseudo random sequence is exclusive ored with 66.66 KHz PCM data to get 1 MHz spread spectrum modulated output.

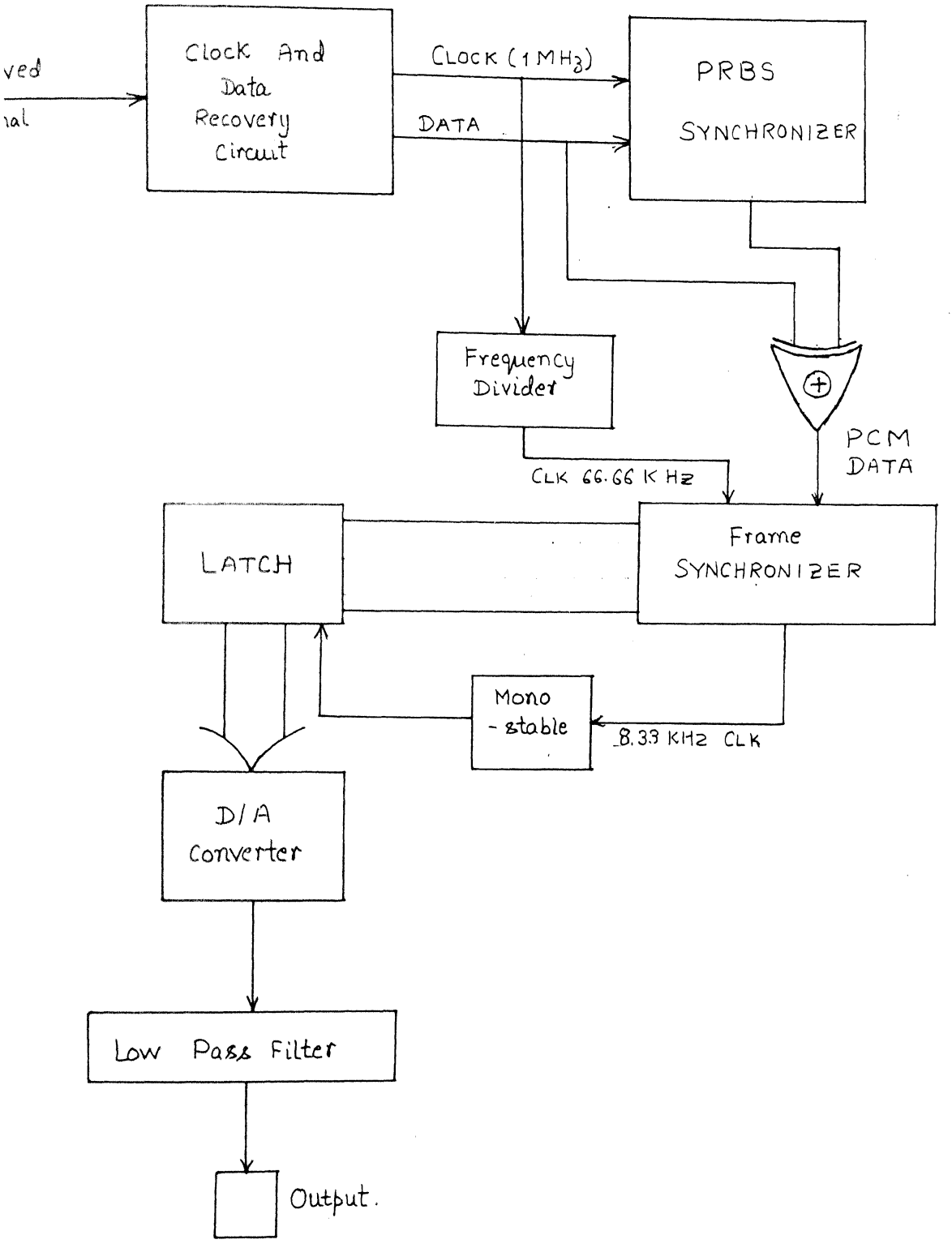

Fig. 4.1: Block diagram of receiver

CHAPTER 4

SPREAD SPECTRUM RECEIVER

4.1 RECEIVER IMPLEMENTATION:

The main function of the receiver is to recover the original information signal from the received data stream (PRBS or its complement). The block schematic is shown in Fig. 4.1.

The phase locked loop extracts the data and clock from the received signal. This regenerated clock and data are fed to PRBS synchronization circuit. The PRBS synchronization circuit generates the PRBS similar to that of the transmitter. Now to synchronize the receiver PRBS with respect to transmitter PRBS, the data is suppressed initially i.e. only PRBS is transmitted. In this mode the receiver PRBS is synchronized with transmitter PRBS and after this the transmission of data commences. As the PRBS is synchronized, the regenerated data is EX-ORed with synchronized PRBS to get the pulse code modulated data at the output of PRBS synchronization circuit. After this, data is fed to frame synchronizer circuit which provides 7 bit data to latch for information extraction. In case the proper synch bit is existing in data, the frame

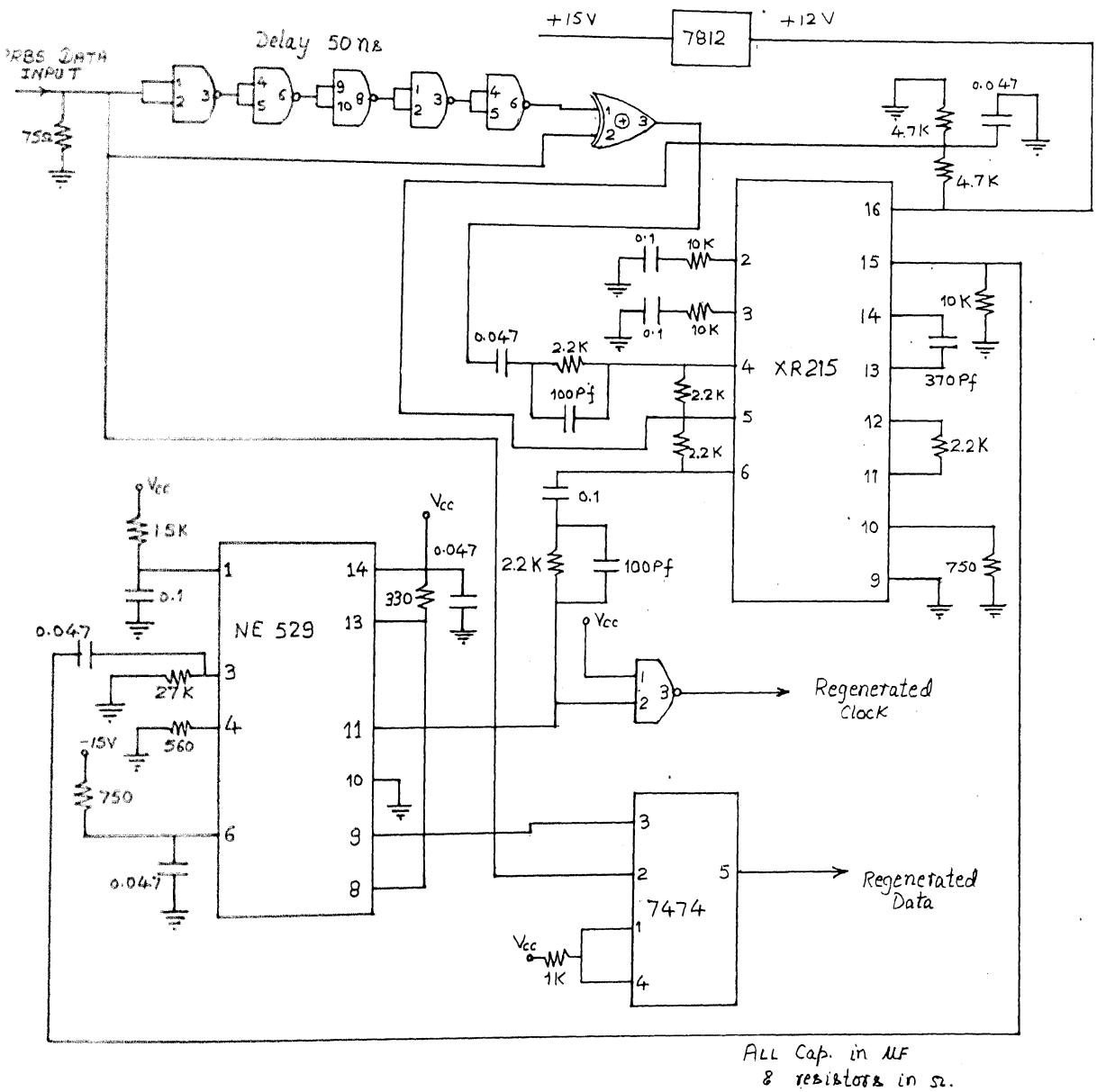

Fig. 4.2: Clock and Data recovery circuit

synchronizer circuit provides 8.33 KHz clock to monostable. This circuit is robust for small amounts of error and it is able to synch again in case of clock failure. The monostable creates enabling pulses for latch and latched information is converted to analog output with the help of D/A converter. The analog output is passed through low pass filter to reject high frequency noise. The description of all the subsystems are as follows.

4.2 CLOCK AND DATA RECOVERY:

The clock and data recovery circuit as shows in Fig. 4.2 consists of XR 215 PLL chip, NE529 a voltage comparator and some MSI digital chips such as 7400 Nand gate, 74S86 high speed EX-OR and 7437 two input Nand buffer etc.

The XR 215 is a highly versatile monolithic phase locked loop system designed for a wide variety of applications in both analog and digital communication systems. It is well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35MHz. It can accommodate analog signals. between 300 micro volts and 3 volts and can interface with conventional DTL, TTL

and ECL logic families. The internal circuit consists of a balanced phase comparator, a highly stable voltage controlled oscillator and a high speed operational amplifier. A self contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low pass filter to the phase comparator output terminals. The VCO section has frequency sweep, on off keying, sync and digital programming capabilities. Its frequency is highly stable and is determined by single external capacitor.

The received signal is delayed for 50 ns by passing it through a series of NAND gates, its delayed output is EX-ORed with direct signal to get the harmonics of clock frequency. This output is fed to pin 4 of PLL after decoupling capacitor and bringing down the signal level to meet the PLL requirement For single supply operation, a resistive bias string as shown in Fig. 4.2 is used to set the bias level at approximately $V_{CC}/2$ at pin 6. The d.c. bias current at these terminals is nominally 8 μ Amps. The phase comparator bias pin 5 should be d.c. biased and a.c. grounded with a bypass capacitor as shown in Figure 4.2. The low frequency voltage across phase comparator output pins 2 and 3 corresponds to the phase difference between the two signals at the phase comparator inputs (pin 4 and 6). The phase comparator outputs are

internally connected to the VCO control terminals. One of the outputs is internally connected to the non-inverting input of the operational amplifier. The low pass filter is achieved by connecting an RC network to the phase comparator outputs. The four filter configurations provided with this chip is shown in Fig. 4.3.

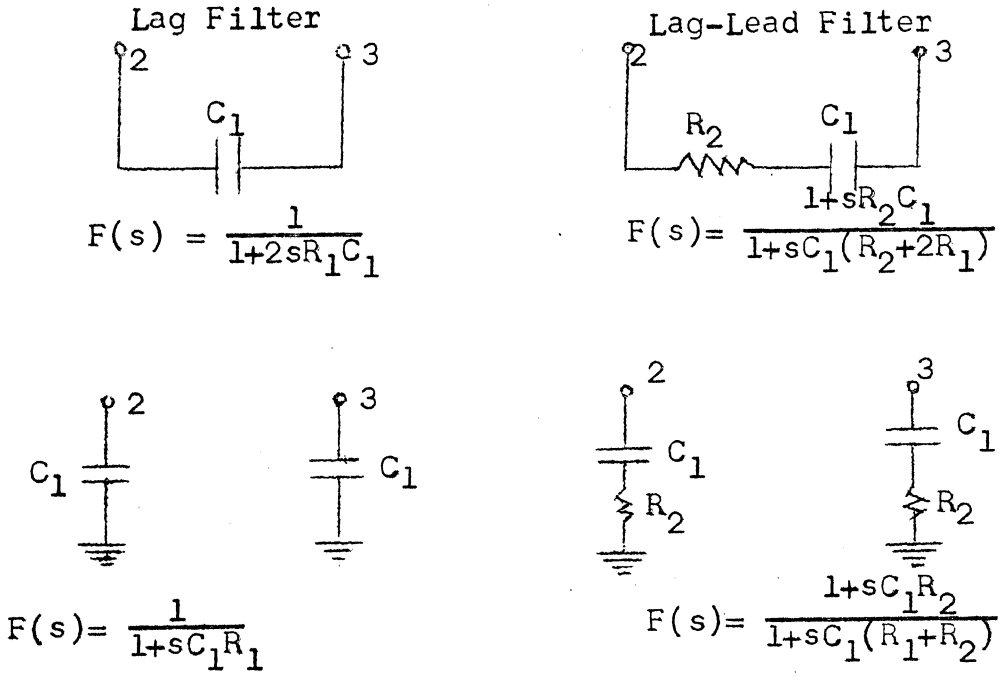

Fig. 4.3: Filter conigurations for XR-215

The filter with the transfer function

$$F(s) = \frac{1 + s\,C_1R_2}{1 + sC_1(R_1+R_2)}$$

was found suitable for the present application. R_2 and C_1 are shown in the Fig. 4.3 and R_1 (6 KΩ) is the internal

impedance at pins 2 and 3 of XR 215. The VCO free running frequency, f_o, is inversely proportional to timing capacitor C_o connected between pins 13 and 14. A 370 pf timing capacitor is connected to set the VCO at 1 MHz. The VCO produces approximately a 2.5 volts peak to peak output signal and the d.c. output level is approximately 2 volts below V_{CC}. The pin 15 is connected to pin 9 through a 10K resistor to increase the output current drive capability. The VCO voltage to frequency conversion gain is determined by the choice of timing capacitor C_o and gain control R_o (2.2K) connected externally across pins 11 and 12. The frequency range of XR 215 is extended by connecting a 750 Ω resistor across pins 9 and 10. As operational amplifier is not used pins 1, 7 and 8 are left unused.

Now to convert PLL output to digital level, a very fast voltage comparator NE 529 is used at its output. One of the main features of the device is that supply voltages (V_1^+, V_1^-) need not be balanced. However negative supply (V_1^-) should always be at least five volts more negative than the ground terminal. Input common mode range should be limited to values of two volts less than the supply voltages. (V_1^+ and V_1^-) upto a maximum of ± 6 volts as supply voltages are

increased. It is also important that output A is in phase with input A, and output B is in phase with input B. As shown in Fig. 4.2, input A and output A have been used for clock recovery, while output B is fed to the clock pin of 7474 (D flip flop) for data recovery. The frequency output of NE 529 pin 11 is fed back to one of the phase comparator inputs of XR 215. At the output stage, a buffer driver is provided for protecting the NE 529 from getting overloaded. The received data is retimed with the clock to get regenerated data.

4.3 PRBS SYNCHRONIZATION:

The main purpose of this block is to synchronize receiver regenerated PRBS with the transmitter PRBS. In this circuit a 74194 4 bit bidirectional universal shift register, a 74164 8 bit parallel output serial register and some TTL ICs such as 7400, 7474, 7486 and 7432 are used as shown in Fig. 4.4.

For PRBS synchronization, initially the data is suppressed at the transmitted i.e. only PRBS is transmitted. This circuit takes only four clock pulses to synchronize with the transmitter PRBS. The 74164 is a 8 bit shift register with asynchronous clear. The gated serial input A and B (pin 1 and 2) permit complete control over incoming data, as

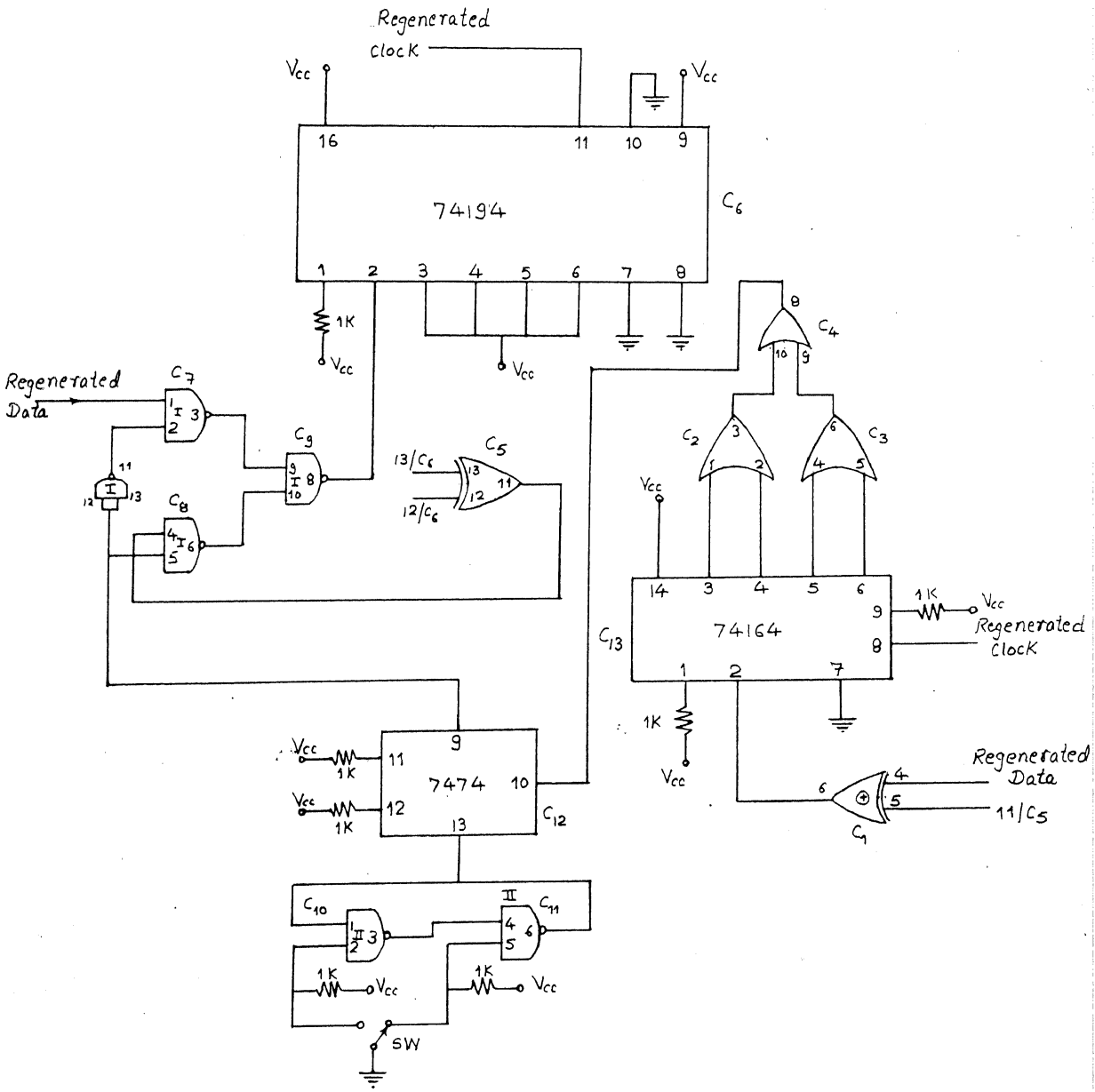

Fig. 4.4: PRBS Synchronizer

a low at either (or both) inputs inhibits entry of new data and results the first flip flop to the low level at the next clock pulse, A high level input enables the other input which will then determine the state of the first flip flop. The clocking occurs on the low to high level transition of the clock input.

In 74164 (C_{13}) one of the input pins is kept high (pin 1), pin 2 gets output of C1 EX-OR. The input pins of C1 EX-OR are connected to regenerated data from clock recovery circuit (initially transmitted PRBS) and locally generated PRBS (i.e. pin 11 of C5). In fact C1 checks for the PRBS synchronization. The C13 (74164) and C6 (74194) get one MHz clock from clock recovery circuit. As explained in transmitter PRBS generation scheme, pin 11 of C5 generates PRBS. The circuit components C7, C8 and C9 acts as multiplexer and depending upon C12 output (pin 9), the locally generated PRBS or transmitted PRBS is passed to pin 2 of C6. At the output of C13 (74164) three OR gates (C2, C3 and C4) are provided to detect all zeros states. If the transmitted and locally generated PRBS are perfectly matched, the pin 2 of C13 gets string of zeros and the output pins 3,4,5 and 6 of C13 go low and hence the decoder circuit consisting of C2, C3 and C4 also create a low level which sets the C12. Otherwise also if

there is any mismatch between the two PRBS's, pin 2 of C13 gets subsequent high and low level and in turn the flip flop C12 gets set. And so in both the cases the locally generated PRBS is passing through C6. Now to synchronize this PRBS, the flip flop C12 is reset with the help of C10 and C11 and an external switch which create a low level at the reset pin 13 of flip flop.

As soon as C12 is set, within 4 clock pulses, the synchronization occurs because the transmitted PRBS is forced to pass through the C6 i.e. 4 bit shift register. After synchronization again the C12 is reset and locally generated PRBS resumes. Now after the synchronization is achieved, the actual data transmission starts. If the EX-OR C1 is analyzed now, its output produces the pulse code modulated data at 66.66 KHz similar to that of the transmitter. This data is further taken to frame synchronization for information extraction. It may be recalled here again that for PRBS synchronization, we have to follow a drill that initially only PRBS is transmitted for a very short duration i.e. 4 μsecs. (duration of four clock pulses).

4.4 FRAME SYNCHRONIZATION:

As shown in Fig. 4.5 frame synchronization or data synchronization circuit provides exact 7 bits data to latch

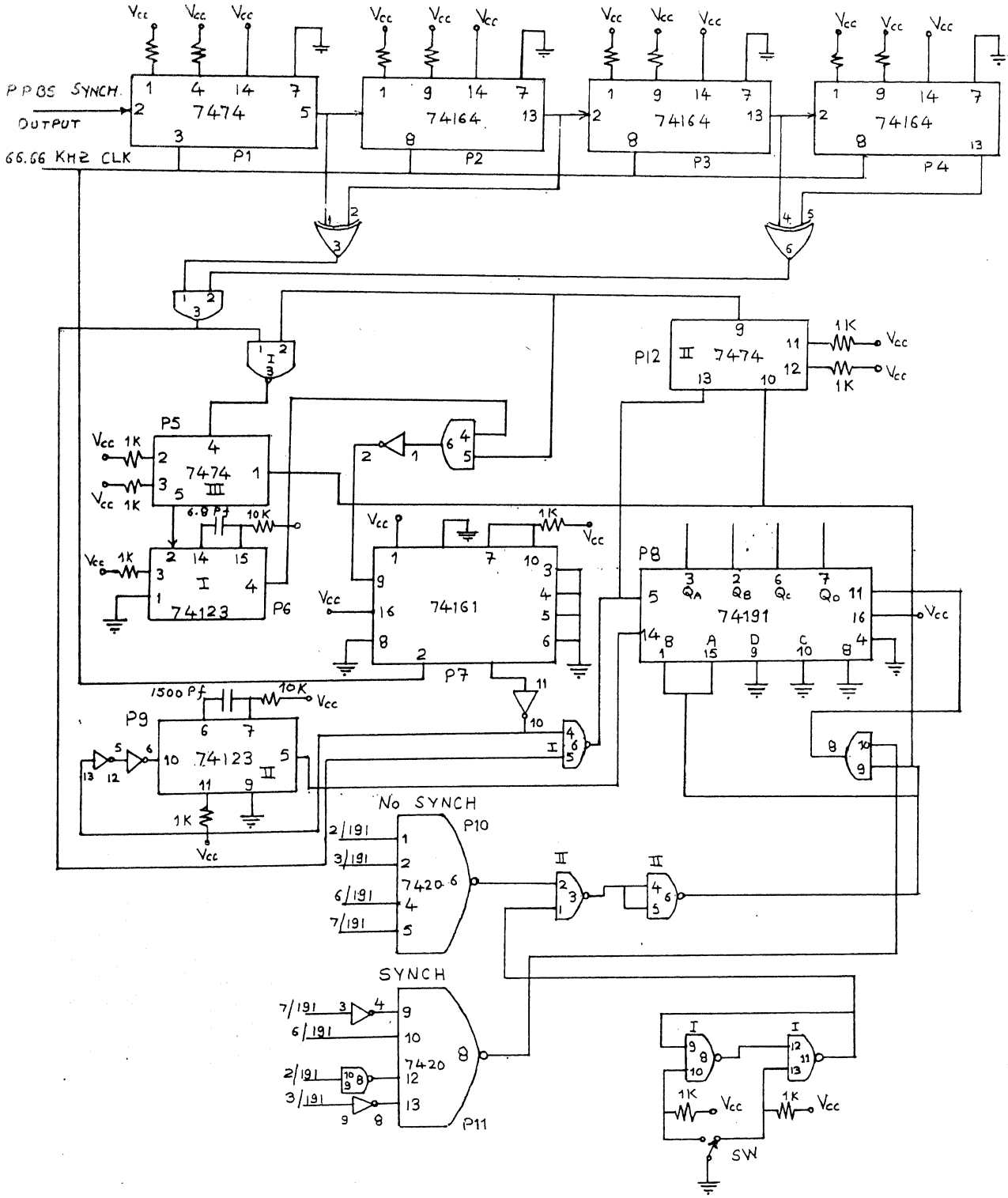

Fig. 4.5: Frame Synchronizer

for information extraction. It is robust for small errors in data and able to synch. again in case of clock failure. After clock recovery circuit a divide by fifteen counter is provided for getting 66.66 KHz clock frequency. This clock is connected to a D flip flop (P1) which is used as shifting device and a series of 74164 (P2, P3 and P4, 8 bit parallel output serial shift register). These shift registers alongwith D flip flop are used for extraction of synch. bit with the help of EX-ORs and AND gate which produces output for alternate one's and zero's added in transmitted data as synchronizing bit. As the external switch is operated which is provided for start of operation, the II F/F (P12) gets set. Now the synch. pulse is transferred to III F/F (P5) and this also gets set. The first 74123 (P6) is used as positive edge triggered monostable which creates a clearing pulse to 74161 (P7) and so 74161 (P7) starts counting at the proper edge of the synch pulse. Now this clock and synch pulse are passed through NAND gate to reset the II F/F (P12). After the II F/F (P12) gets reset, the synch bits are not passed on by I (123) NAND gate and frame synchronization exists as long as the synch bit is received properly.

The 74191 (P8) binary synchronous up down counter is provided for small amounts of errors in the channel. Whenever

the synch exists, the 74191 is in up counting mode and stable state is 3. Suppose there is any error in the channel i.e. the synch bit is missing, then it starts counting down to zero and if still the error exists, it searches for new synch by setting the II F/F. So it can account for maximum three countinuous slipping of synch bits. Hence if there is small error then it counts down to zero and again comes back to its stable state of three in synch mode. There are two decoder circuits for decoding 15 and 4. The decoder 15 works in no synch mode and decoder 4 comes in picture in synch mode. In brief the transition stages may be written as follows:

Synch mode (up count) $0 \longrightarrow 1 \longrightarrow 2 \longrightarrow 3 \longrightarrow 4$ stable state 3

No synch mode (down count) $3 \longrightarrow 2 \longrightarrow 1 \longrightarrow 0 \longrightarrow 15$ stable state 0

4.5 LATCH AND D/A CONVERSION:

This circuit receives the synchronized data as well as the clock from frame synchronizer circuit and latches the whole information for digital to analog conversion. As shown

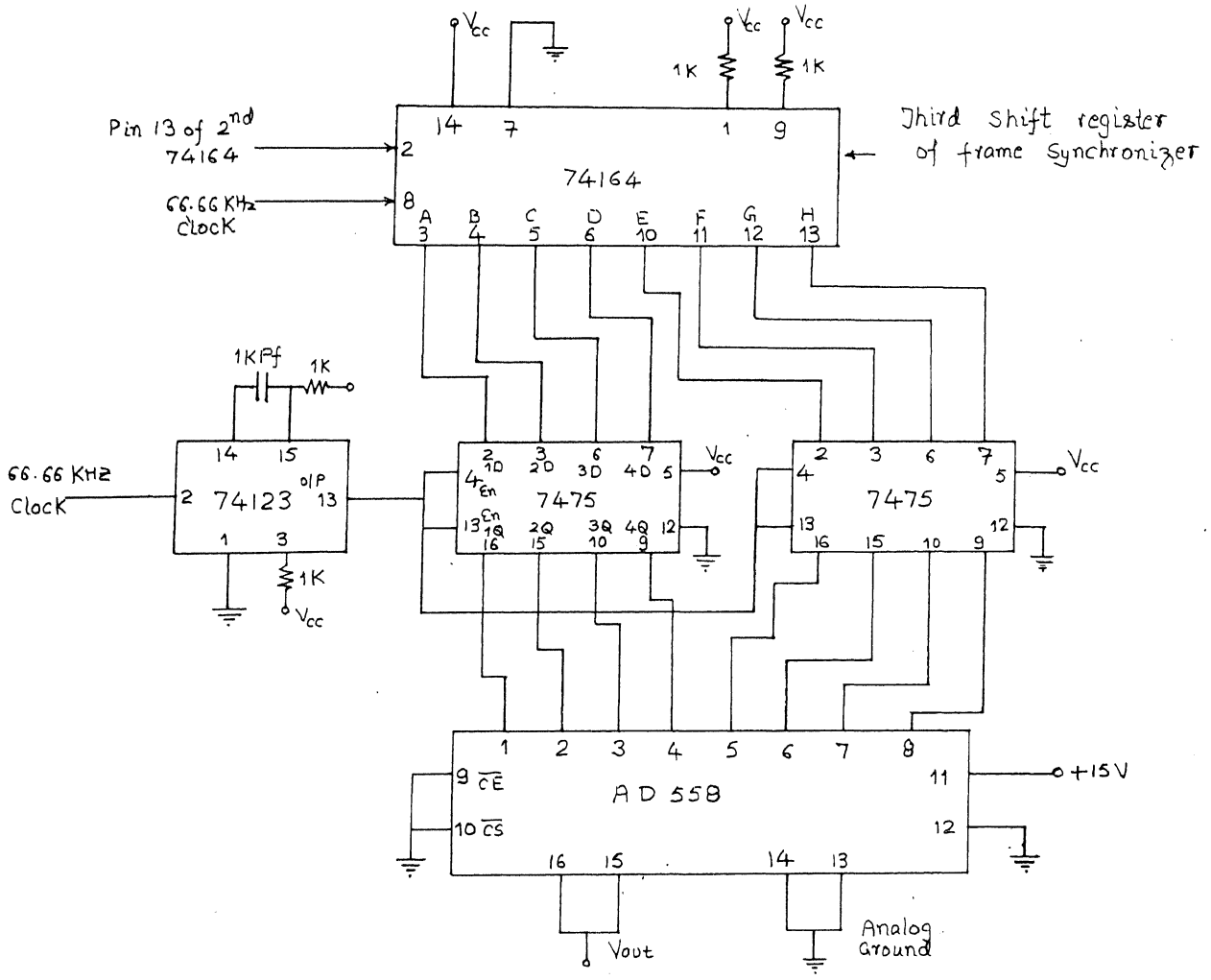

Fig. 4.6: Latch and D/A Converter

CHAPTER 5

CONCLUSION

In the present work a SSM system is designed and fabricated. Information signal (0-4) KHz bandwidth is pulse code modulated and expanded using 15 bit PRBS. A simpler scheme is adopted for frame synchronization by adding a synch. bit in the PCM data itself at the transmitter stage. The system has been fabricated using readily available IC chips.

Even if three bits in the fifteen bit PRBS are received in error, the receiver corrects them from the knowledge of the correct 15 bit PRBS. Similarly even if there are three consecutive errors in the synch. pulses, the receiver performs the frame synchronization correctly. The performance of the receiver was tested by directly feeding the transmitter output and was found satisfactory. The receiver PRBS synchronization takes only 4 micro seconds to synchronize with the transmitter PRBS.

The following steps are suggested for fault diagnosis:-

i) A test signal i.e. saw tooth waveform may be generated using counter and D/A converter. In the transmitter itself a D/A converter may be used to check the working of level shifter, sample and hold and A/D converter.

ii) Similarly serial to parallel circuit may also be developed to check the PCM output on closed loop basis.

iii) As the PN sequence is 15 bit long, spread spectrum modulator output can easily be checked on storage oscilloscope.

iv) For receiver circuitry, a small circuit is proposed in Fig. 5.1. This circuit simulates the data low or high with the synch. bit depending upon whether the output inverter is used or not. The receiver output may be verified using this test signal.

v) The PRBS synchronization circuit can separately be checked. For checking this circuit, the input data is suppressed i.e. only PRBS is fed, now as PRBS synchronization switch is operated, the receiver regenerated PRBS gets synchronized with trans. PRBS.

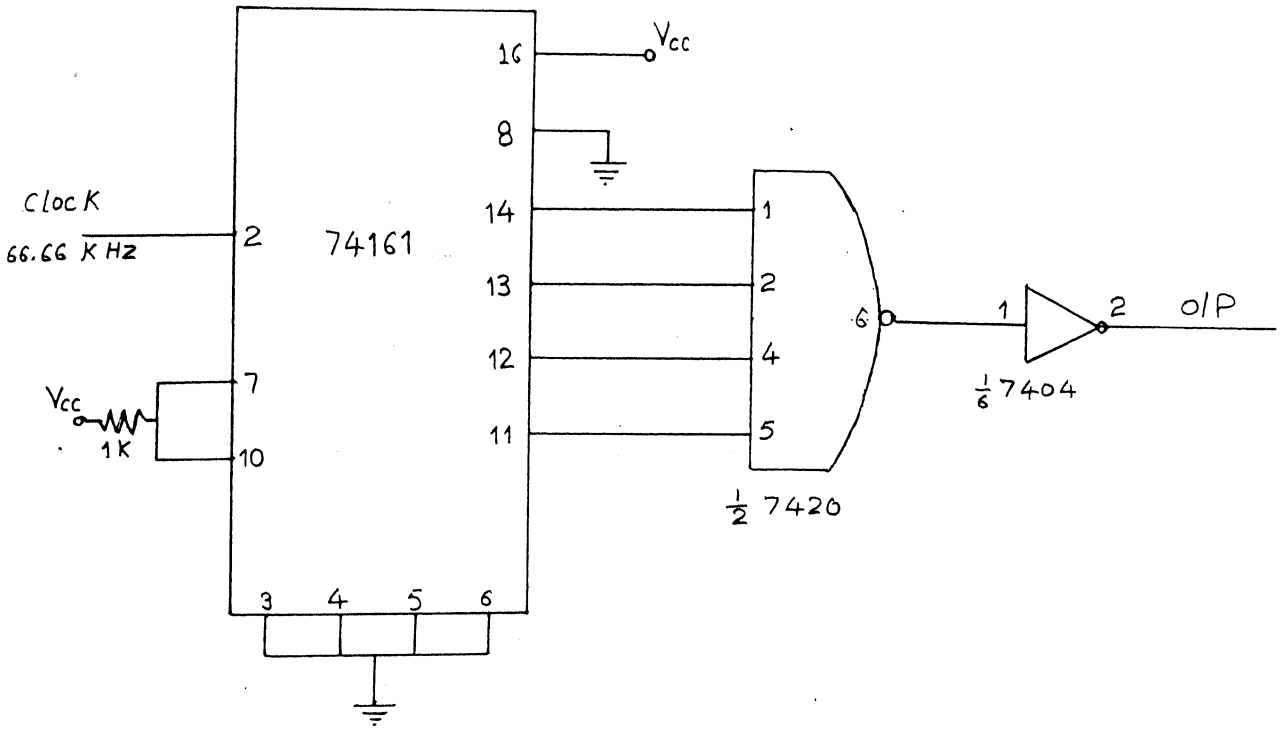

Fig. 5.1: Receiver test circuit

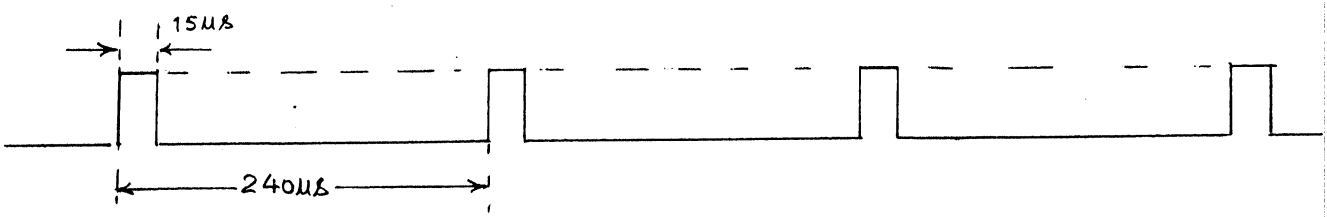

Fig. 5.1(a): Data low with synch bit

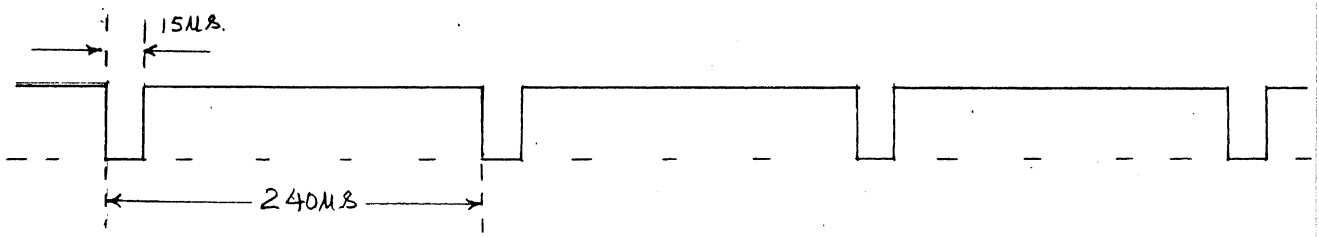

Fig. 5.1(b): Data high with synch bit

The present work may be extended by providing proper power stages and analog modulation to check the system performance in noisy environment and its jamming margin capabilities. The error correcting code may be added in PCM data to improve the system performance.

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